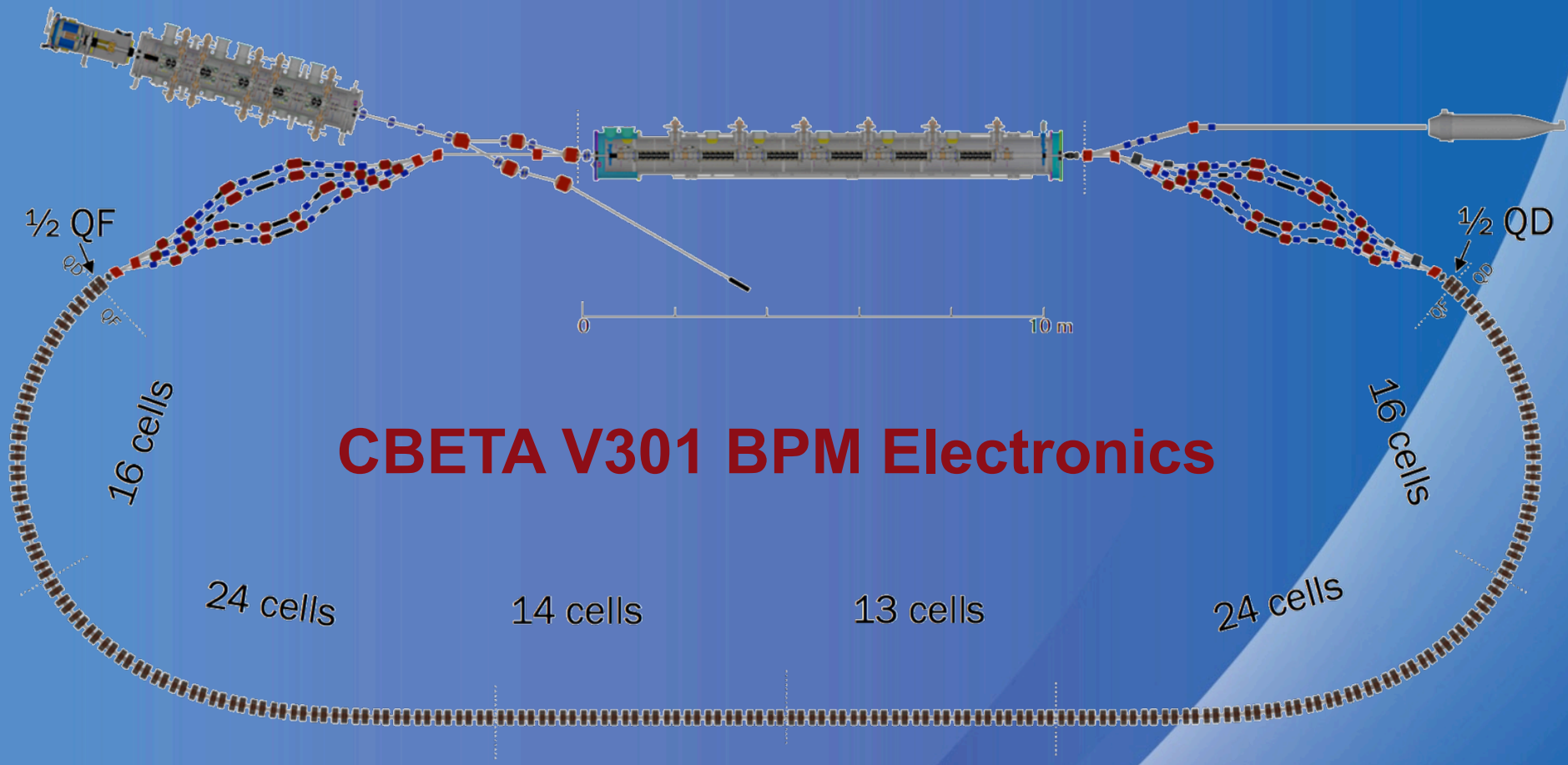


CBETA V301 BPM Electronics

Rob Michnoff, Rob Hulsart, Zach Sorrell,
Adam Bartnik, John Dobbins, Colwyn Gulliford

Advisory Committee Meeting, Feb. 22, 2018

Cornell Laboratory for
Accelerator-based Sciences and
Education (CLASSE)

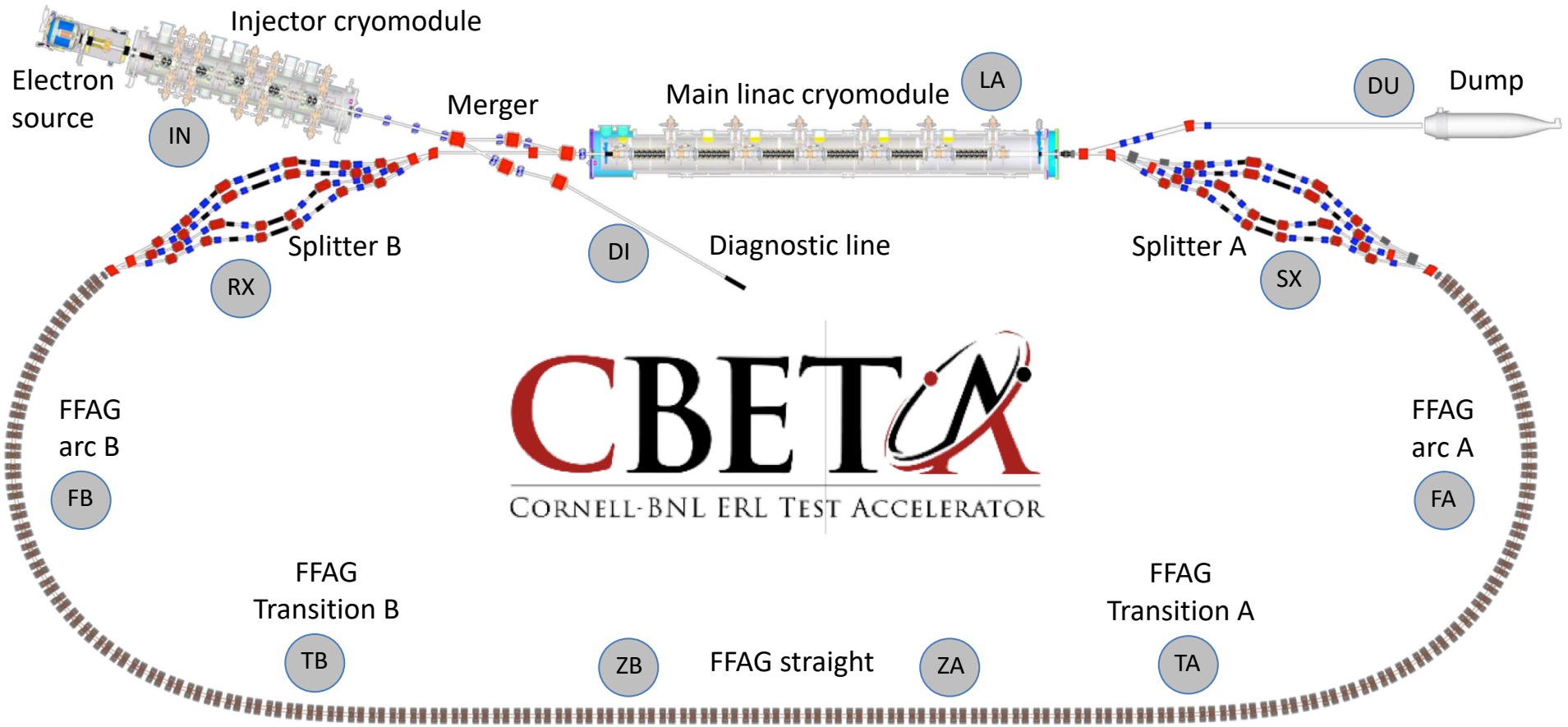
BROOKHAVEN
NATIONAL LABORATORY
a passion for discovery

Office of Science
U.S. DEPARTMENT OF ENERGY

Outline

- The plan
- Status
- Beam tests to date
- Summary

CBETA Machine Layout



CBETA BPM Plan

- ~140 Beam Position Monitor (BPM) modules using BNL designed V301 VME-based hardware module
  - BPM analog to digital converters (ADC) will be timed to the peak of the selected energy bunch, and will compute position based on single raw data sample. Many measurements will be averaged.
  - BPMs will measure one energy beam at a time and will sequence through the different energies by changing beam trigger timing.

CBETA BAM Plan

- 16 Beam Arrival Monitor (BAM) modules using V301 module and CU designed RF mixer chassis
  - BAMs will be used for energy measurements in each of the 8 splitter lines.
  - BAMs will use 2 dedicated BPM buttons in each splitter line – the first and last.

Bunch pattern

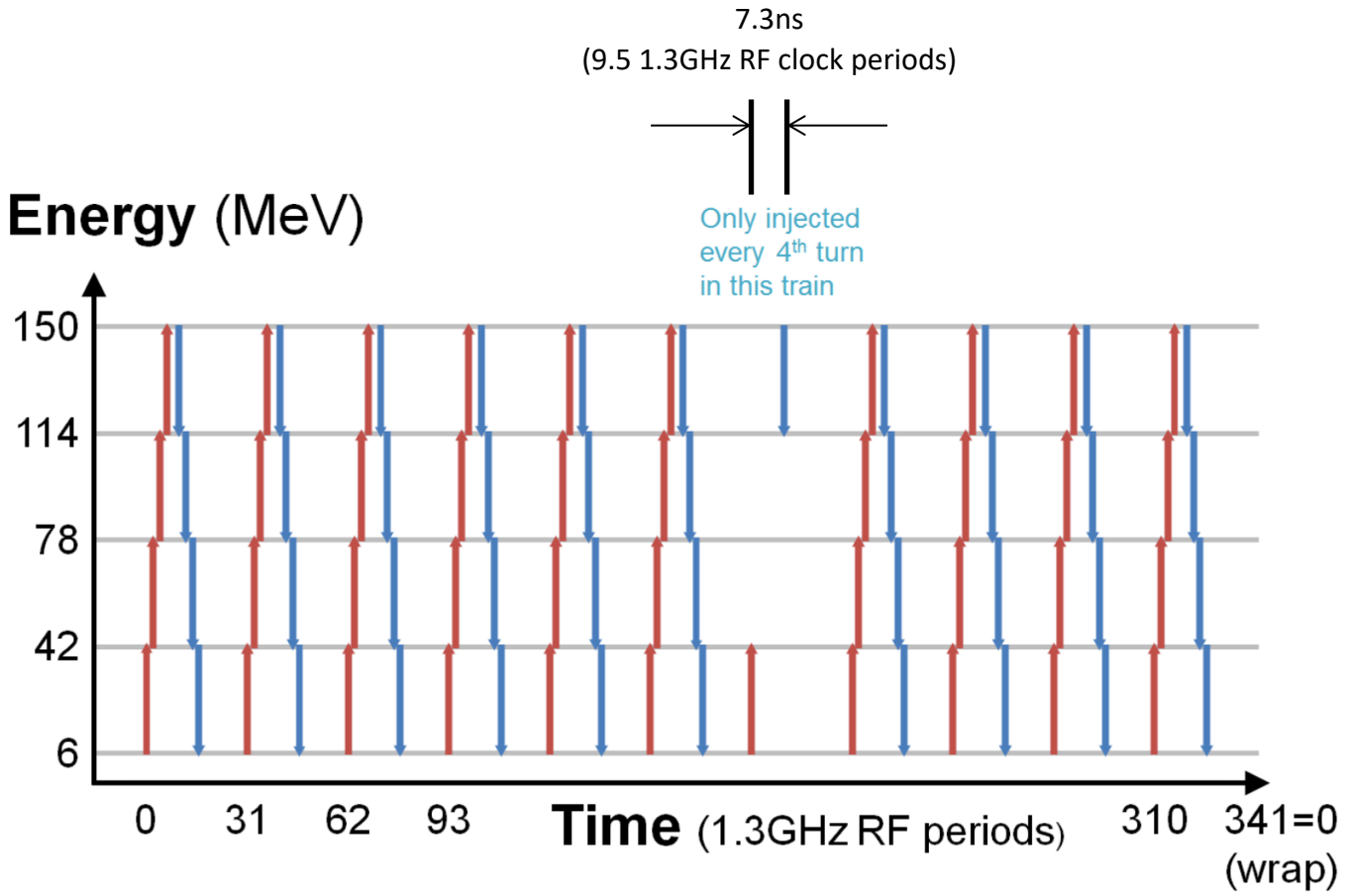


Figure 2.8.1: Bunch pattern produced in the eRHIC-like mode that has a circumference of $h = 343$ RF wavelengths but a time periodicity of 341 RF periods.

Figure from CBETA design report

Bunch pattern

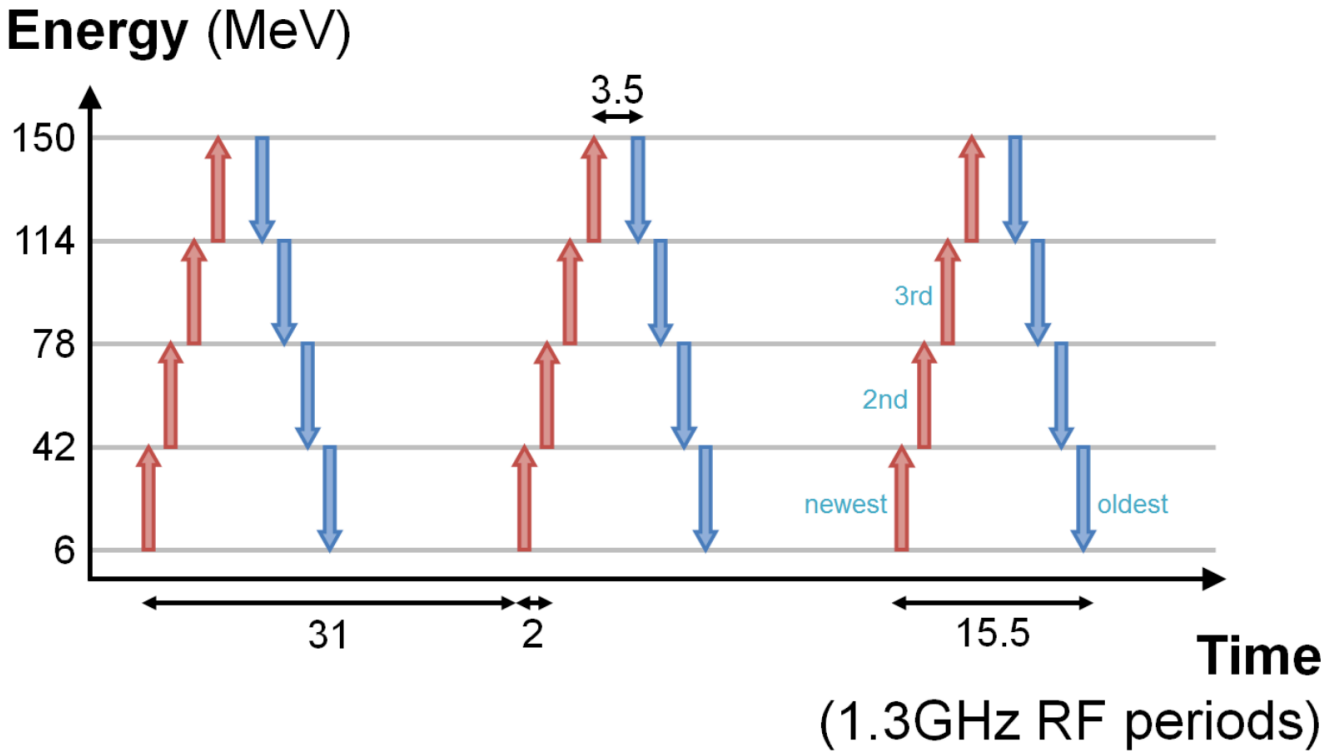


Figure 2.8.2: Bunch train details in the eRHIC-like mode. Note the top-energy bunches are well-separated (by 3.5 RF wavelengths).

Figure from CBETA design report

Status

- Fractional arc test
  - 15 V301 existing BNL modules have been modified with Bessel filter and inductor change
- One-pass and four-pass machine
  - 160 V301 modules are in the process of being procured by BNL for full turnkey PC board assembly

Status

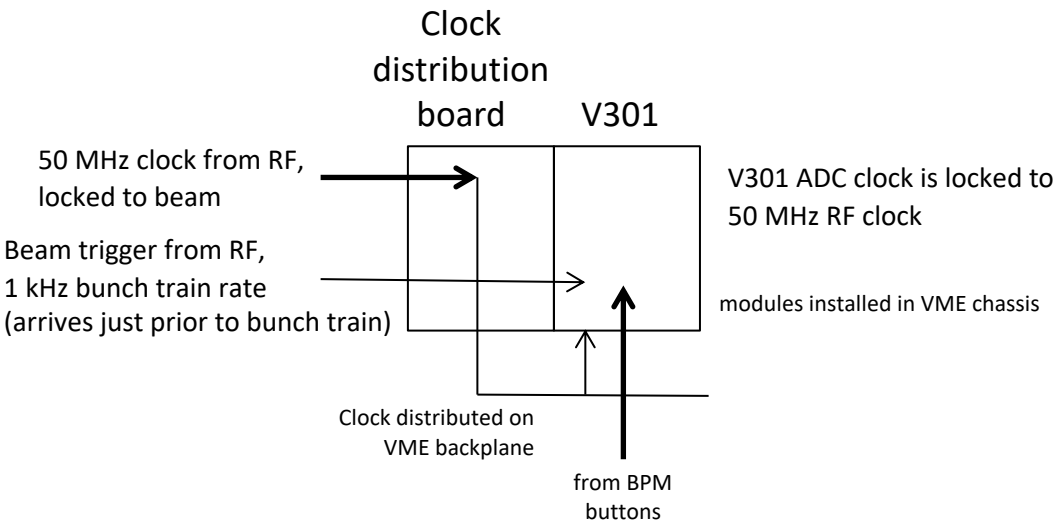
- Locking the Cornell generated 50 MHz RF clock to the V301 BPM module to align the ADC clock to the bunch peak has proven to be very stable
- V301 EPICS IOC has been written and reliably used for beam tests
- CS-studio GUI screens have been developed to control and monitor the V301 modules
- BNL custom-designed clock interface module will be used to distribute the machine RF clock and bunch trigger via the VME backplane

V301 beam tests to date

- Beam tests were performed in
  - December 2016
  - June 2017
  - October 2017
- The beam tests, especially in October 2017 provide solid evidence that we have a viable plan.

Hardware configuration for acquiring button data with single sample at peak of each bunch

(For beam tests performed in June and October 2017)

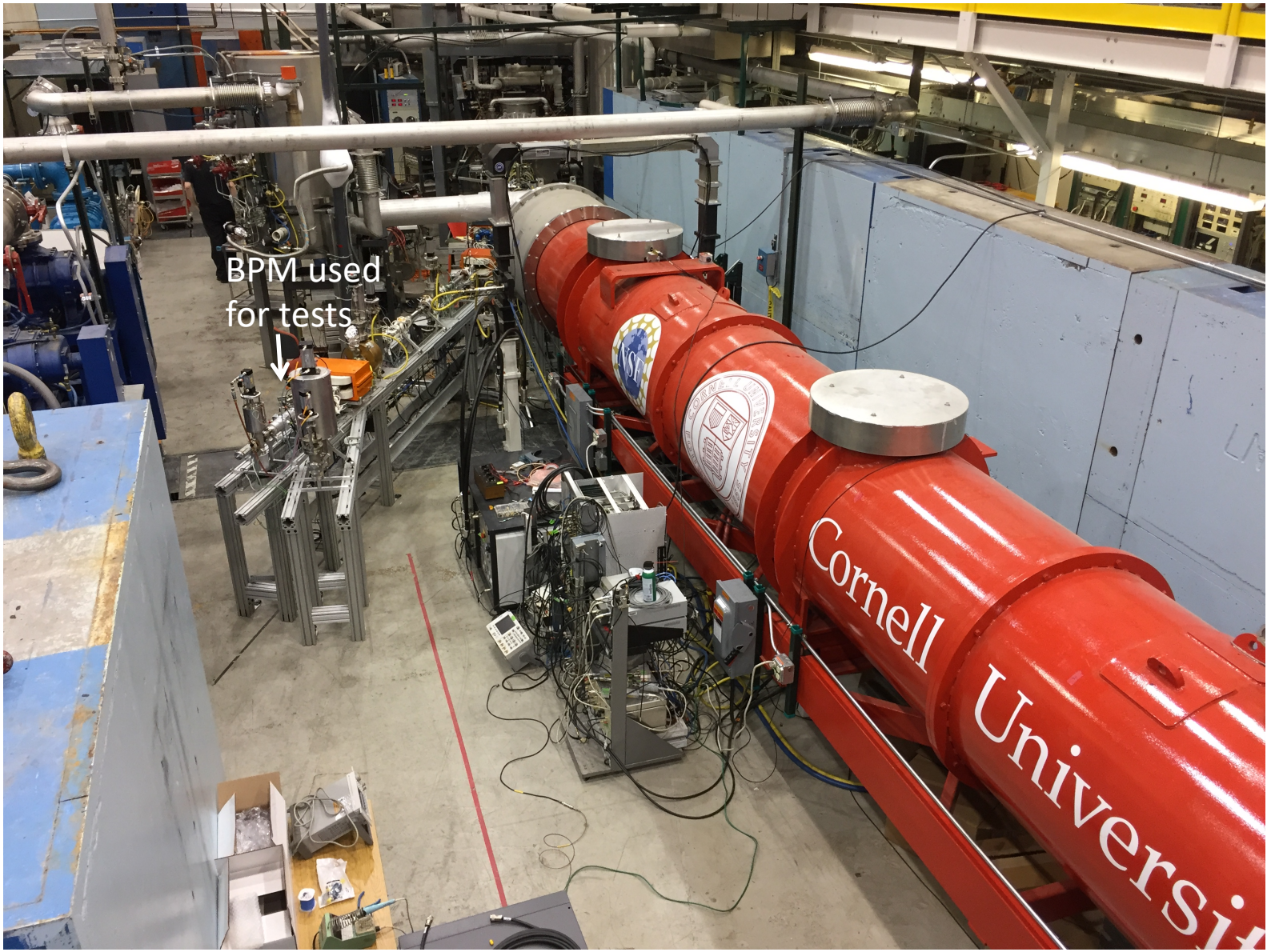


Description of technique for measuring position at the peak of each bunch:

- The 50 MHz beam synchronous RF clock is distributed to V301 module via VME backplane through the V208 module
- The 50 MHz RF clock is multiplied up to 400 MHz in a PLL in the V301 module
- ADC data is acquired using the 400 MHz clock that is locked to the RF 50 MHz clock
- A beam trigger signal from the RF system is used to initiate acquisition of the raw ADC data

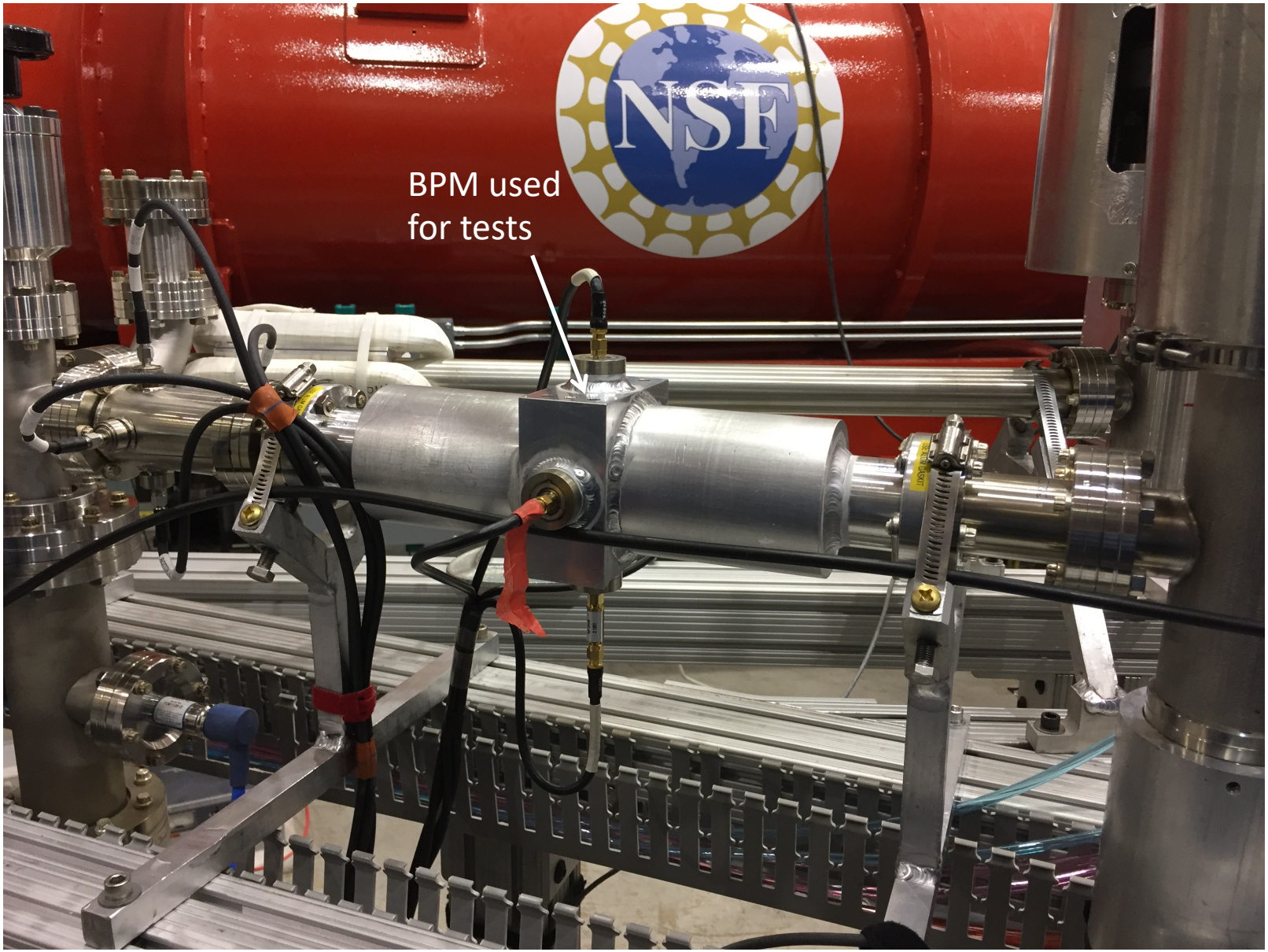
Hardware Setup

(June 2017, October 2017)

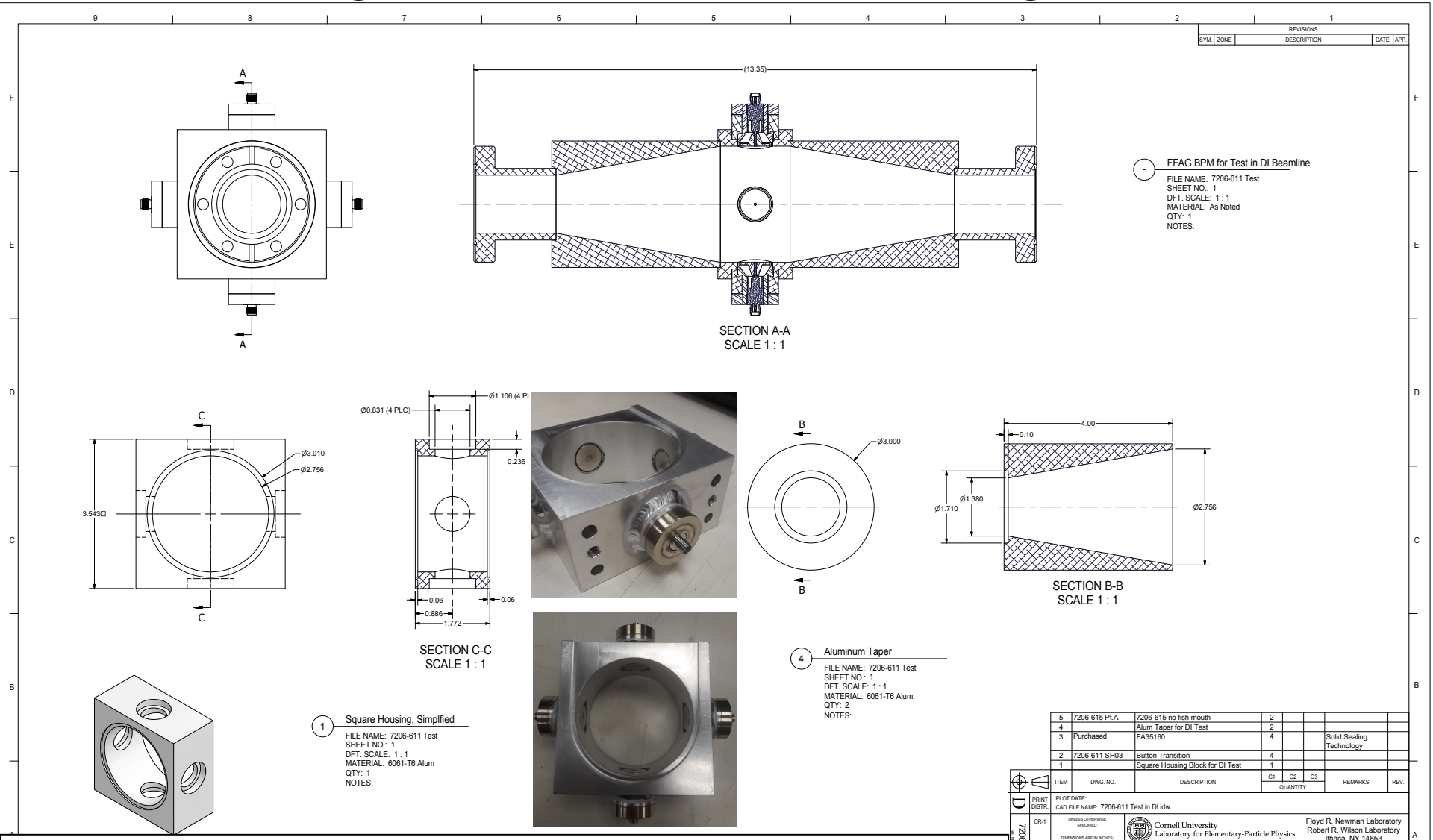


Hardware Setup

(June 2017, October 2017)



Drawing of FFAG BPM installed in diagnostic line



Button diameter: 20 mm

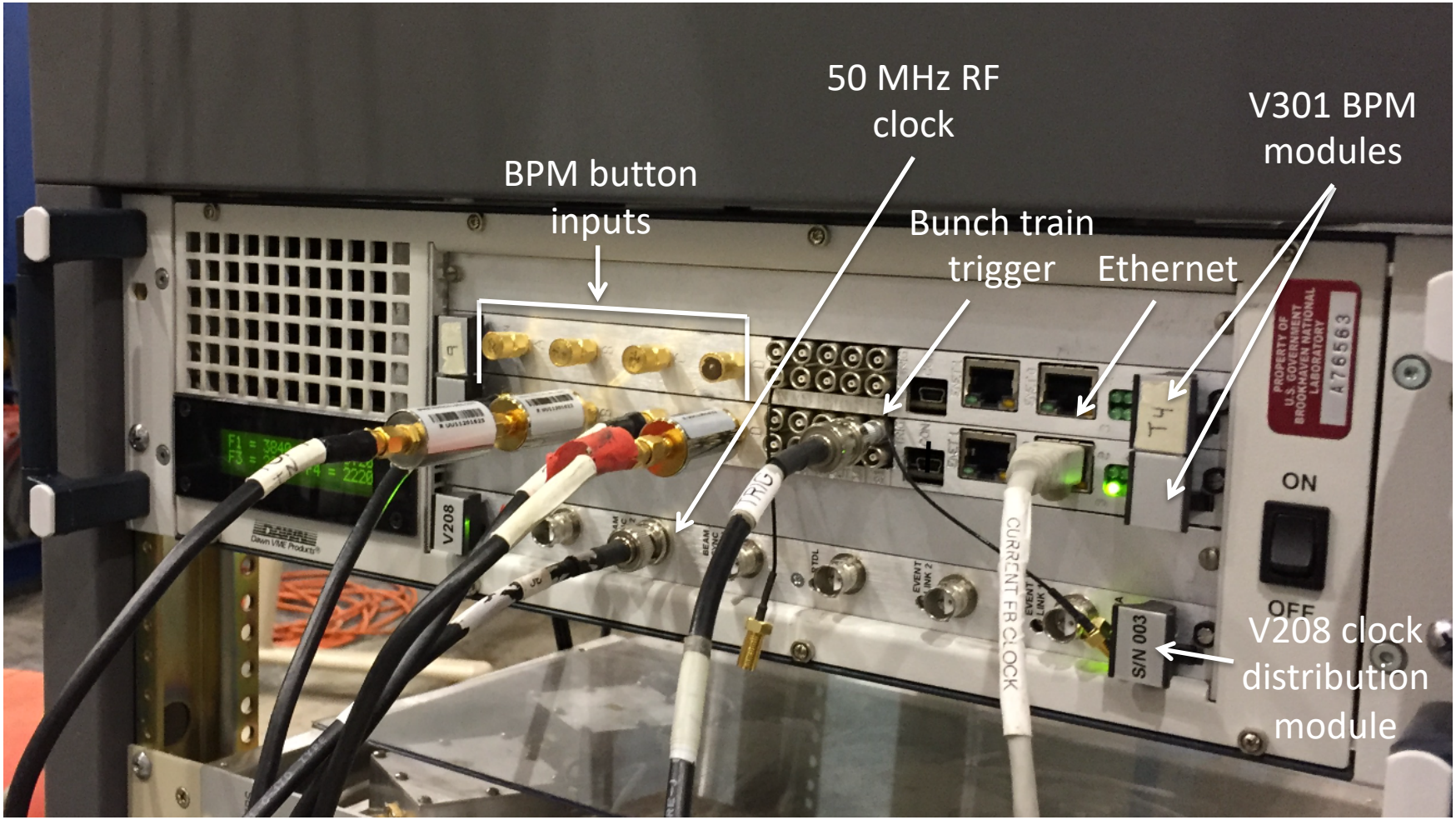
Diagnostic line beam pipe diameter: 1.380 inches (35 mm)

BPM chamber diameter (FFAG beam pipe diameter): 2.756 inches (70 mm)

Expected horizontal beam variations in FFAG: +/-24 mm

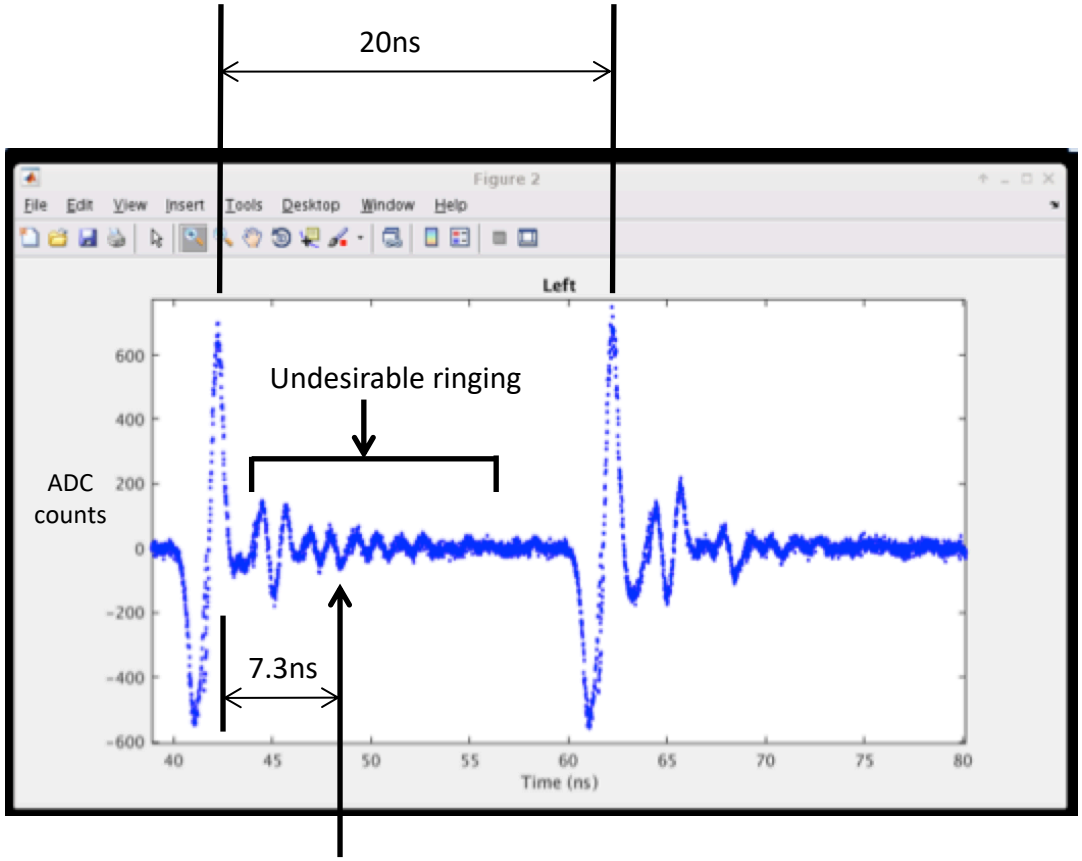
Hardware Setup

(June 2017)



BPM raw beam profile scan with V301

(Beam test results from June 2017)



Location where decelerating energy bunch is expected
(7.3 ns after positive going beam pulse)

Path to reducing signal ringing

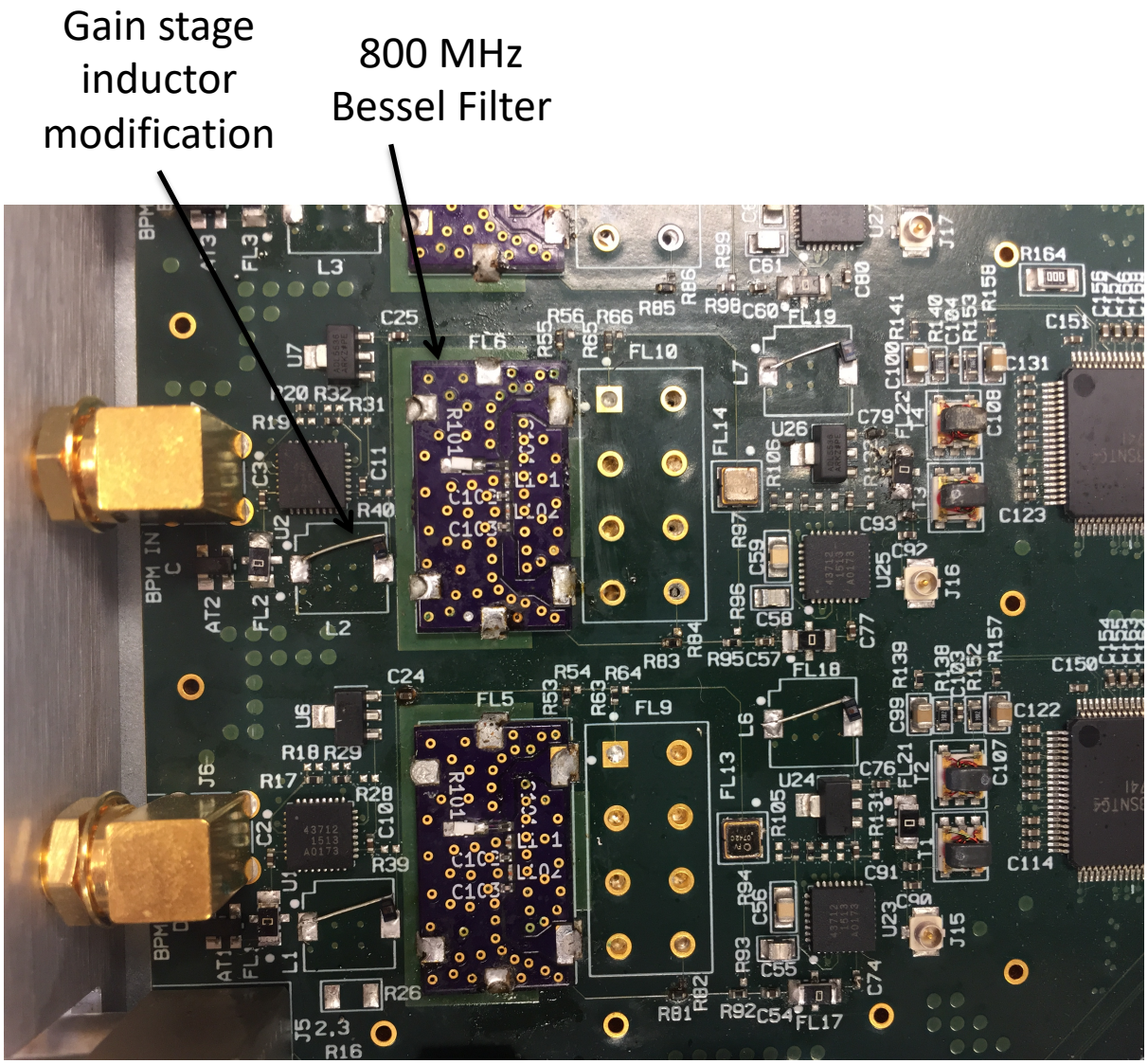
- The main difficulty
  - The electronic response with a simulated signal in the lab is very different from the actual beam
- Reviewed the circuit and developed a set of boards with different options for analysis with beam, including:
  - Replacing the minicircuits LFCN800 800 MHz low-pass filter with a custom Bessel filter, and testing with on-board and external Bessel filter options
  - Testing different inductors on 20 dB gain stages

Hardware Setup

(October 2017)

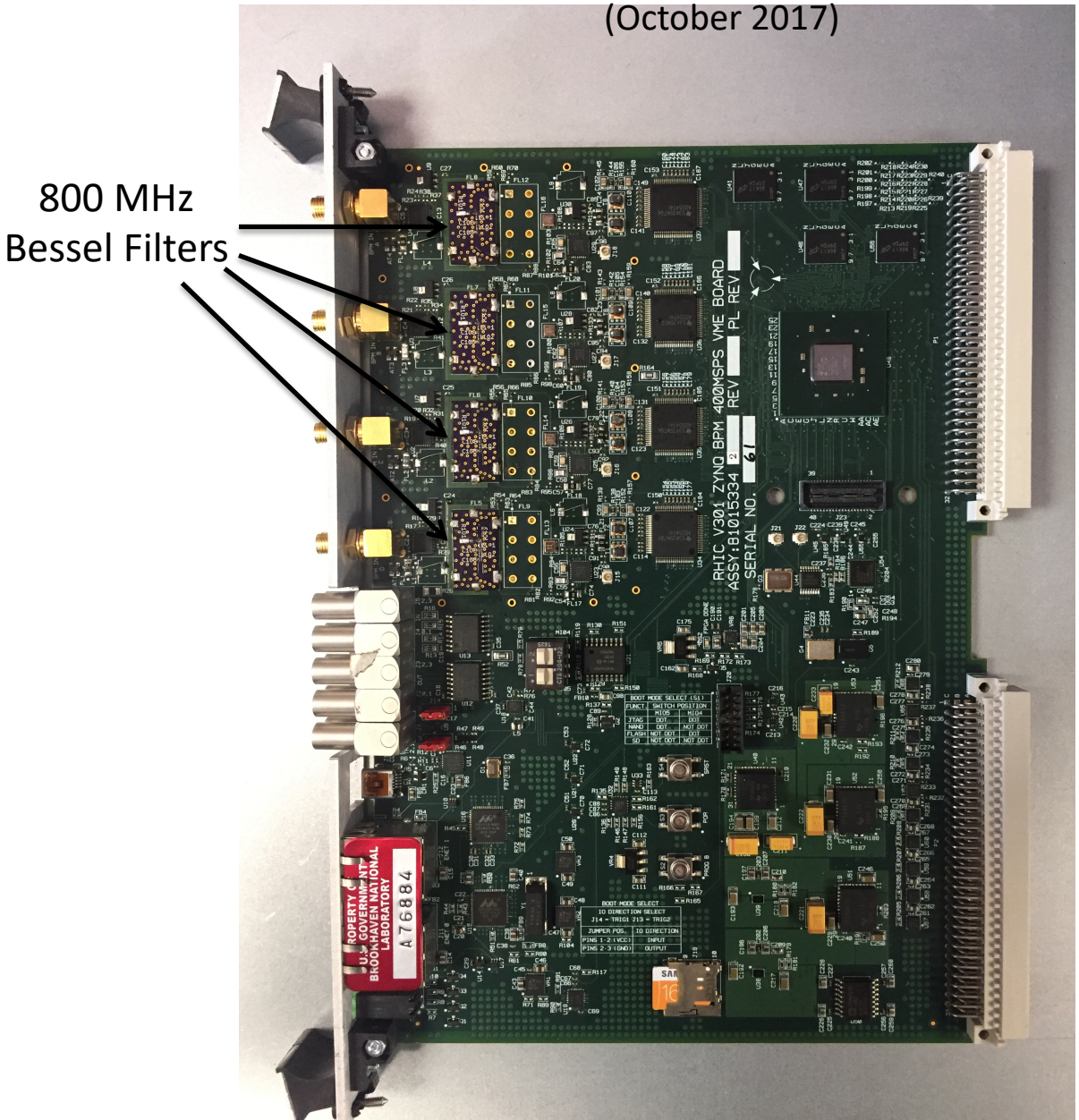
V301 filter and inductor modification

(October 2017)

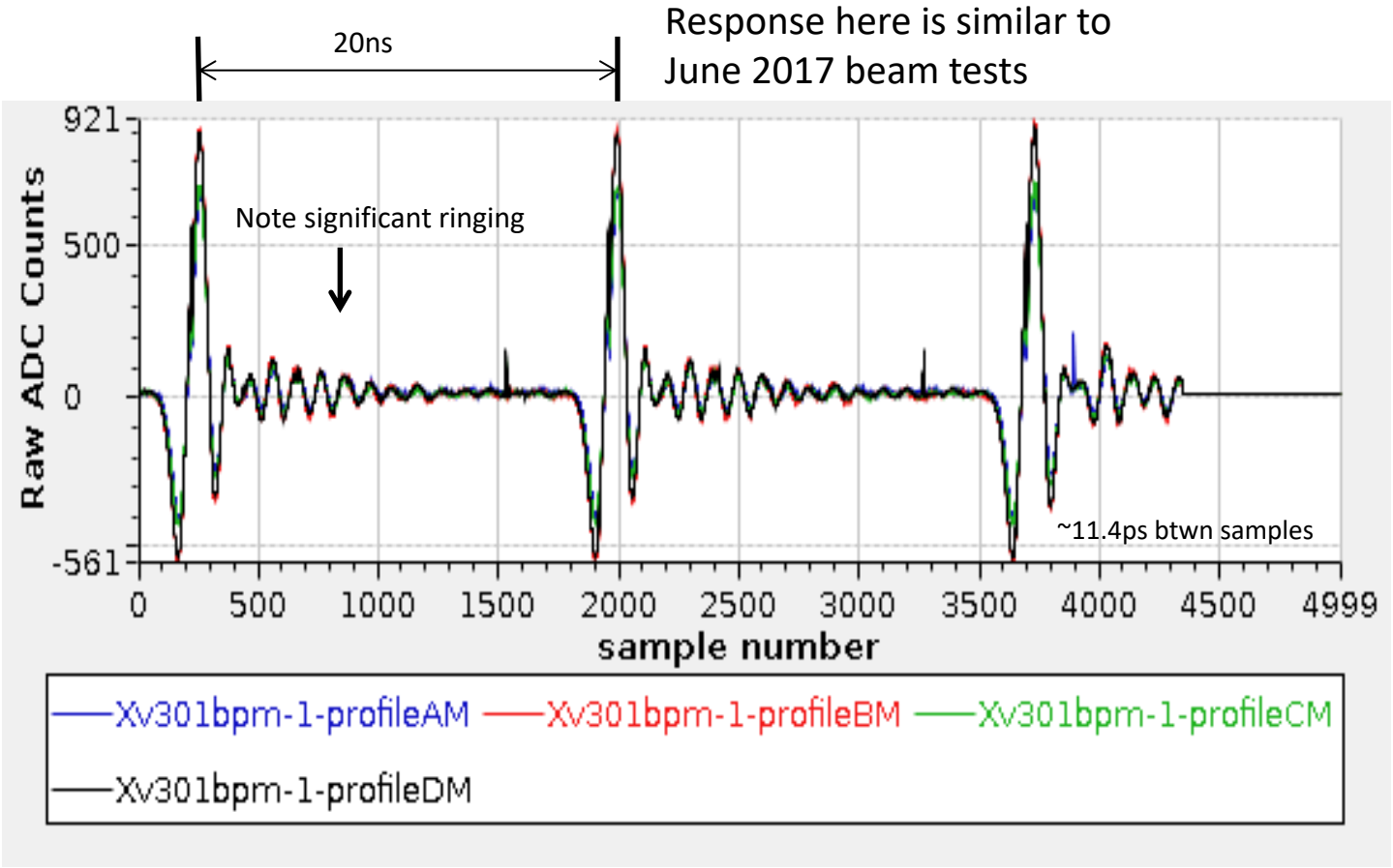


V301 filter and inductor modification

(October 2017)



V301 Beam tests, October 2017
Comparison of BPM raw profile scans



V301 serial #49

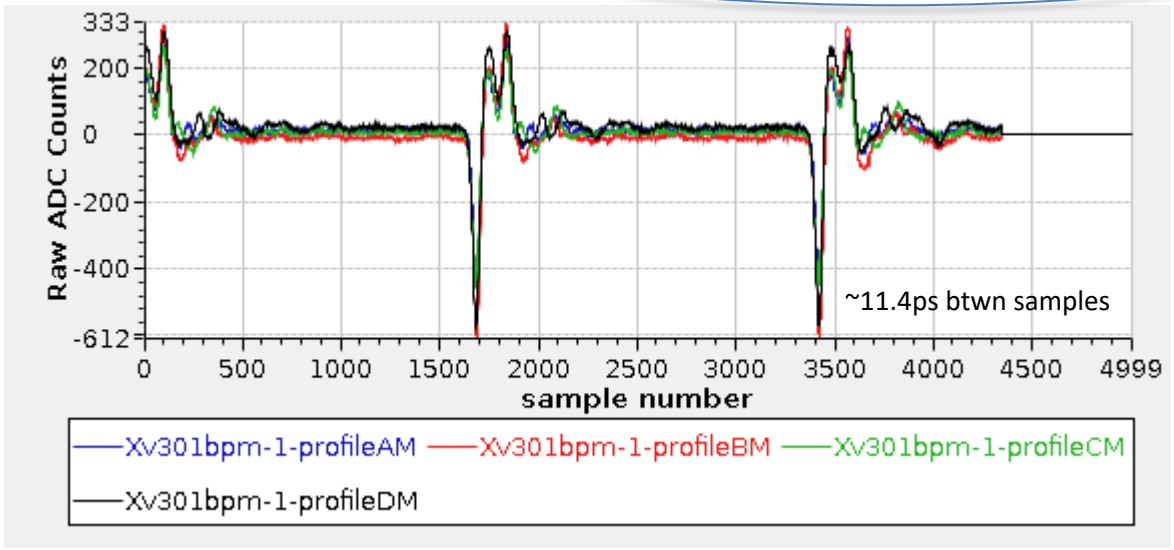
all 4 channels - LFCN-800 filters and Coilcraft 0603 470nH inductor

V301 Beam tests, October 2017
Comparison of BPM raw profile scans

V301 serial #61

All 4 chans - Bessel filter,
Coilcraft 0603 470nH inductors

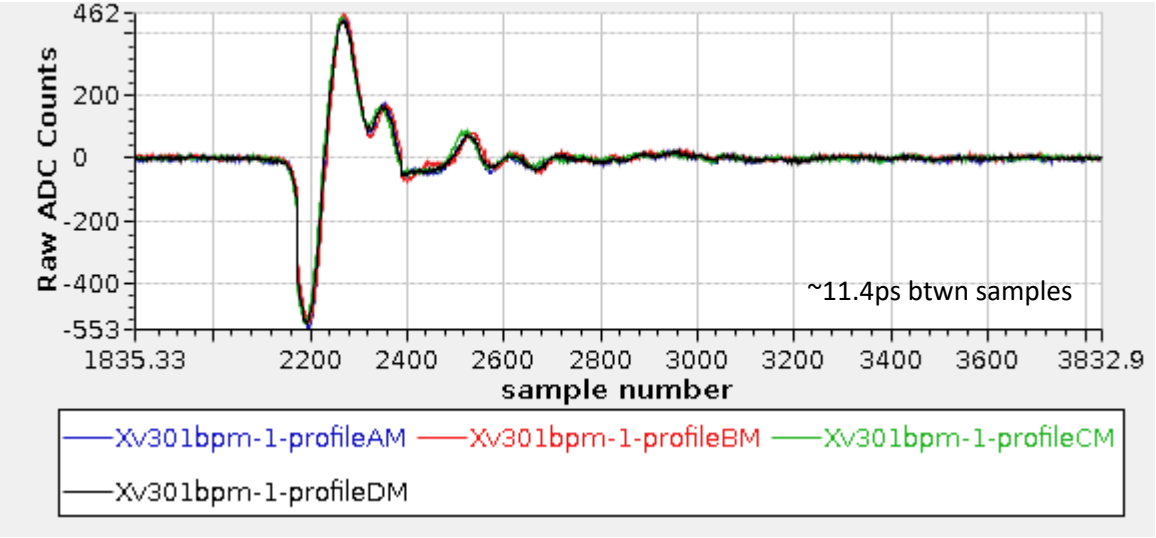
<u>This is the selected configuration</u>



V301 serial #85

all 4 chans - Bessel filter,
7x7mm 470uH inductors

V301 Beam tests, October 2017
Calibration test with beam

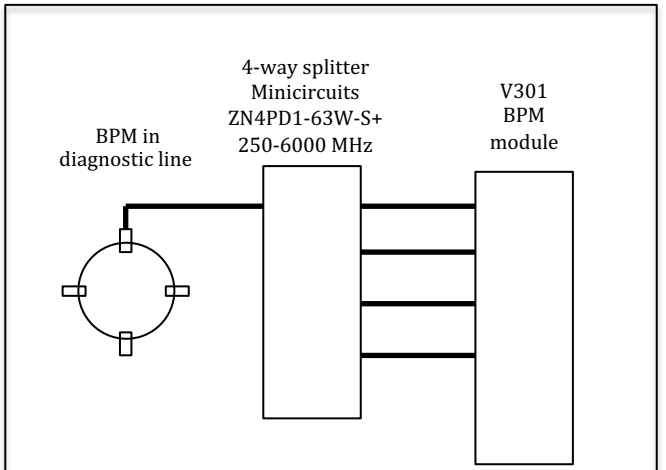


V301 serial #61

All 4 chans - Bessel filter, Coilcraft 0603 470nH inductors

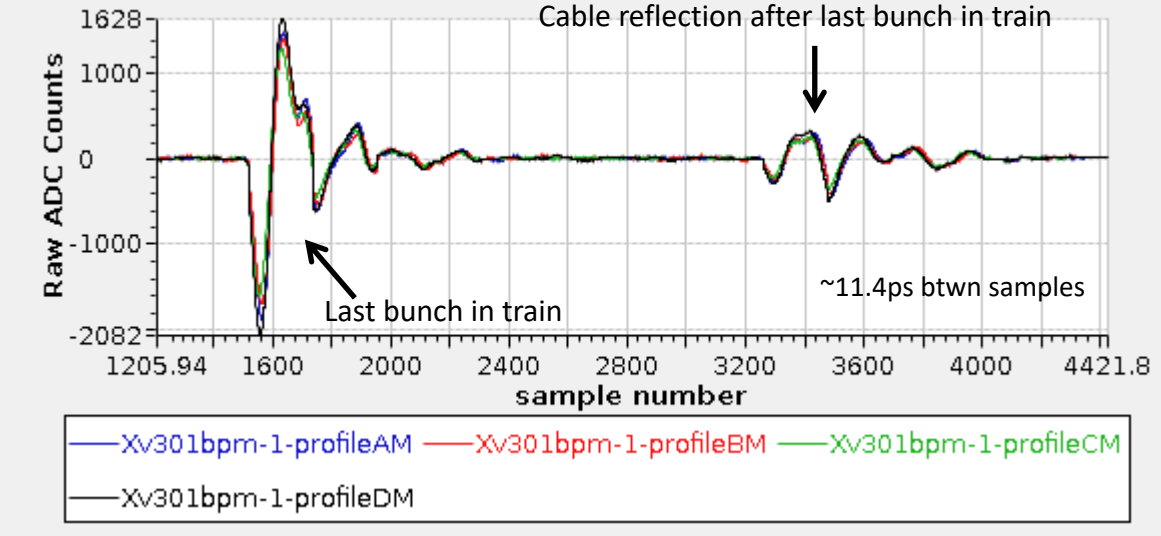
One button connected to 4-way splitter to each input connection

Note that all 4 signals are very well matched when single button is split to all 4 inputs. This is a profile of raw ADC counts with no calibration coefficients applied.



Block diagram of configuration used to calibrate V301 BLM electronics with beam

V301 Beam tests, October 2017
Cable Reflection

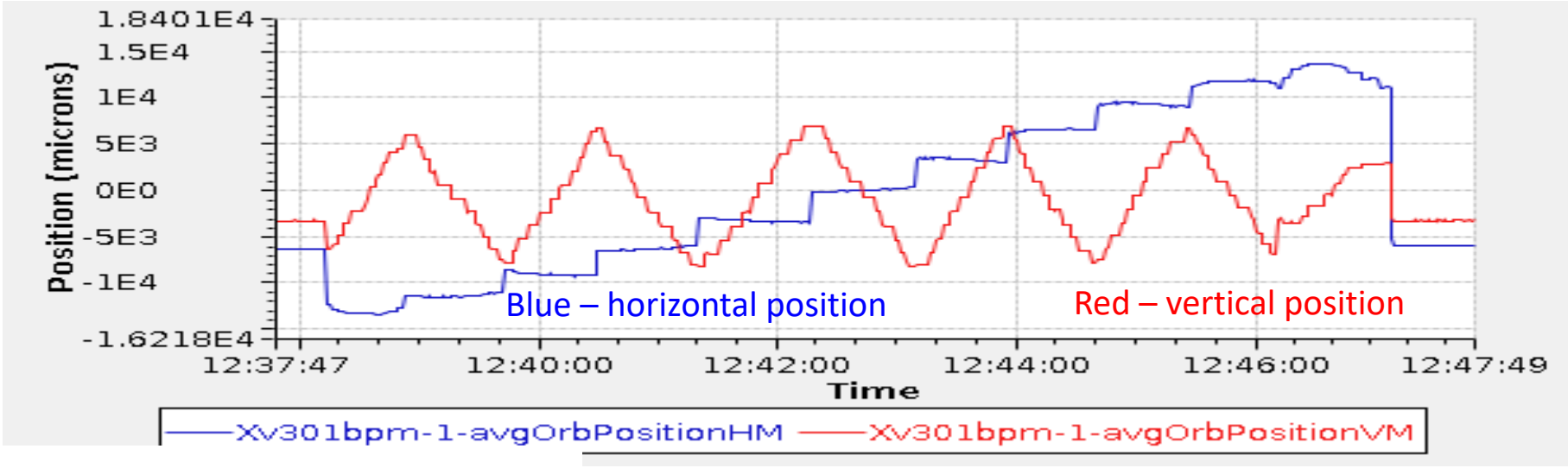


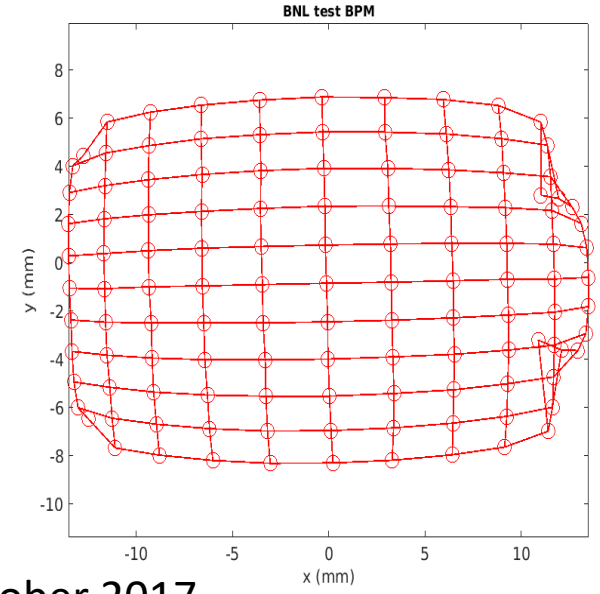
V301 serial #61

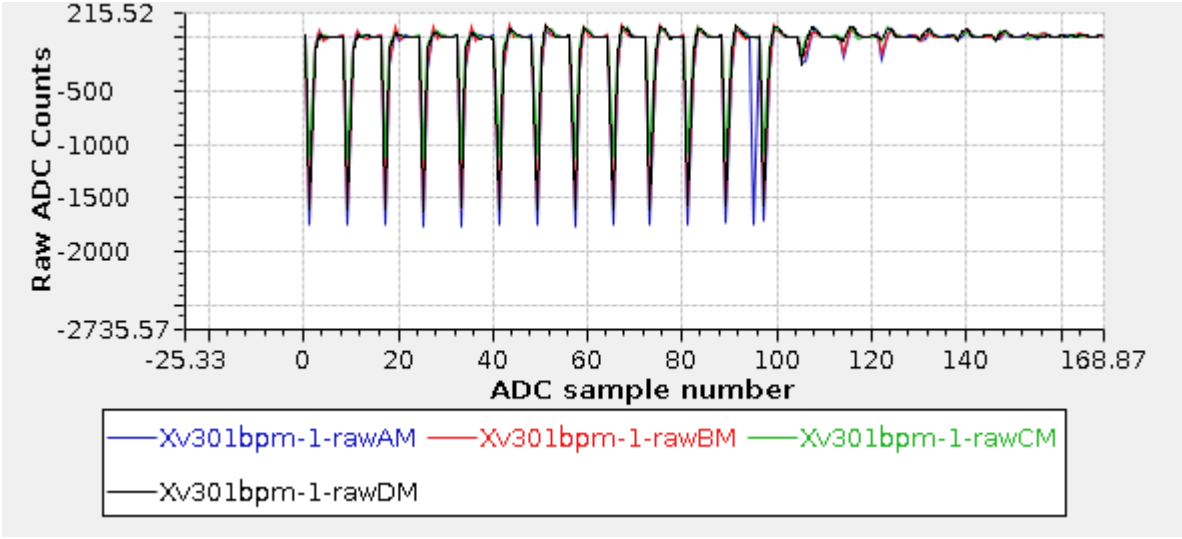
All 4 chans - Bessel filter,
Coilcraft 0603 470nH inductors

BPM cable lengths need to be carefully selected to avoid having reflected beam signal overlap bunch being measured. This may also require adjusting the bunch pattern.

Plots of BPM measurements while scanning the beam horizontally and vertically







October 2017

Summary

- A solid design and plan for providing BPM measurements has been developed and tested with beam
- Measuring different energy beams still presents challenges, but is achievable
- An application for automatically configuring the BPM timing for each energy needs to be developed
- Synchronizing the V301 ADC clock to the RF clock has proven to be very reliable and stable
- The system clock used to derive the ADC clock is presently 50 MHz which is the present bunch repetition rate. This clock will need to be different for the final machine.