Design and Fabrication of a Radiation-Hard 500-MHz Digitizer Using Deep Submicron Technology

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Project Summary

The proposed International Linear Collider (ILC) will use tens of thousands of beam position monitors (BPMs) for precise beam alignment. The signal from each BPM is digitized and processed for feedback control. The demand on the digitizers depends on their location at the accelerator complex. The two large damping rings require the fastest high-precision and high-bandwidth digitizers. We propose to continue the development of the digitizers that were originally designed for the warm linear collider. Although the specification of the digitizers for the ILC is not yet finalized we expect digitizers similar to the one we are designing will be necessary[1].

We propose to continue the design of an 11-bit (effective) digitizer with 500 MHz bandwidth and 2 G samples/s. The digitizer is somewhat beyond the state-of-the-art and hence not commercially available. Moreover we plan to design the digitizer chip using the deep-submicron technology with custom transistors that have proven to be very radiation hard (up to at least 60 Mrad). The custom enclosed layout transistors with guard rings were developed for high-energy physics applications in a very high radiation environment. The design mitigates the need for costly shielding and long cables while providing ready access to the electronics for testing and maintenance. Once a digitizer chip has been successfully developed via several prototype runs, an engineering run at a cost of ~$150,000 will produce all the chips necessary for the ILC, including those BPMs that require less demanding digitizers. We have extensive experience in chip design using Cadence[2]. This proposal was reviewed by the Holtkamp Committee in 2002 and 2003 and awarded, for both years, a rank of 2 on the scale of 1 to 4 with 1 having the highest ranking. This proposal was funded by DOE in FY03 and has been reviewed for three more years, FY04-6. Last year as we prepared to submit a chip with test circuits and a partial ADC circuit we found that IBM had changed the availability of our chosen IC fabrication process (IBM 6HP SiGe BiCMOS), making it unaffordable for us, at roughly 3 times the previous price. This prompted us to change our design to the IBM 5HPE process with 0.35 μm feature size. We request funding for FY07 to continue the design work and submit the first prototype chip. For FY08, we will irradiate the chip to test the radiation hardness and refine the design based on the results from the first prototype chip and submit one more prototype.

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Project Plans

The digitizer chip is very challenging: large bandwidth (500 MHz), high precision (11 bits), and fast sampling speed (2 G samples/s). We capitalize on the experience of our engineering staff that, over the last ten years, has designed radiation hard chips for ATLAS, CLEO III, and CMS. Our most recent design of the DORIC and VDC chips for the ATLAS pixel detector uses the IBM deep submicron technology with feature size of 0.25 μm and enclosed layout transistors to achieve radiation hardness[3]. In addition, we have extensive experience designing fast analog electronics systems such as those used in high-resolution drift chambers.

We propose a 12-bit pipelined digitizer as shown in Fig. 1. In this scheme the input is crudely digitized in the first stage (3-bit cell). The digitized value is then subtracted from the sampled input value, amplified by eight and presented to the second stage. This identical process is repeated for each of the four stages. A one-bit comparator follows the last stage so the final result can be rounded to 12 bits.

The 12-bit digitizer is somewhat beyond the state-of-the-art. However, there is one characteristic of the BPM that may ease the design requirements. The input from each bunch to this system is a sequence of doublets. We currently design the digitizer for a bunch spacing of 1.4 ns. The bunch spacing is expected to be somewhat larger for the dumping rings of the ILC and this will improve the feasibility of the project. Only one parameter is needed to completely specify a doublet. Thus the requirements could be met with a digitizer sampling at the bunch frequency (1/1.4ns or 714 MHz). By interleaving three digitizers, we can have a chip with 2 G samples/s to provide more redundancy. In the following, we first discuss the required precision of some of the circuits in the digitizer and then the control of the errors in order to achieve the desired precision.

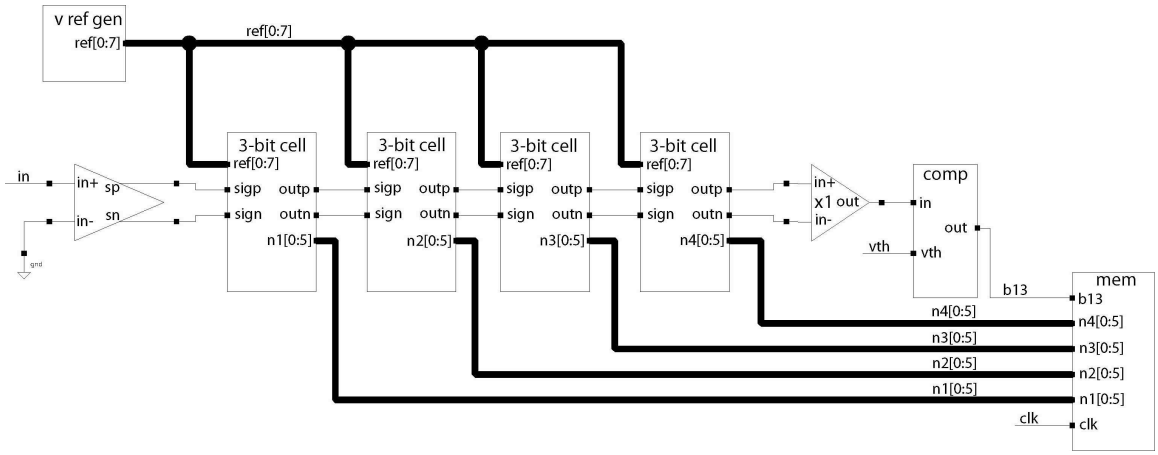

Figure 1. Schematic of a 12-bit pipelined digitizer.

Precision

Submicron CMOS does not allow large power supply voltages, 2.5 V is common. This limits the internal signal swing. We can estimate the necessary precision by assuming that

a 3 V full scale range can be achieved for the differential internal signals. This means the LSB is 3 V/4096 or 732 μV. Thus comparator thresholds must be stable and accurate to one half the LSB or 366 μV. Amplifier and sample/hold gains must be stable and accurate to about the same precision, 0.01% (~ 0.5/4096) of full scale. Charge injection errors in the sample/hold circuits must also be controlled to the same level of precision.

Error Control

There are three types of errors in the digitizer:
1. Offset errors: uncertainties in the comparator thresholds, fixed charge injection from the sample/hold, and amplifier offset.
2. Gain errors: uncertainties in the gain stages and sample/hold gain.
3. Dynamic errors: uncertainties in the timing and amplifier and sample/hold settling times.

Offset and Gain errors will be measured as part of the qualification test on raw chips. These errors do not have to be measured individually. For example the offset error from the comparator, the charge injection offset and amplifier offset will be measured as a single number. These values will be loaded into an on-chip memory. The raw digitized numbers will be used only as indices to tables of "correct values", which will be used to calculate the true input value. The maximum number of these calibration values is estimated to be 72. With this scheme, we only require stability in the design and process. Based on experience, this level of stability should be achievable over a modest temperature range. In addition these devices can be recalibrated in the field.

Dynamic errors will be controlled by careful design. By means of simulation and prototyping we will design each of the internal functions to have sufficient bandwidth to settle in the required time.

Process

The proposed digitizer requires several amplifiers with a gain of eight. Let us assume that we allow half the bunch period (0.7 ns) to sample and the other half to hold. To settle to 12 bits with a precision of one half the LSB requires nine time constants ($e^{-9} \sim 0.5/2^{12}$) or a rise time of 171 ps (2.2τ with $\tau = 700$ ps/9). To accomplish this the fabrication process must provide a product of gain (8) and bandwidth ($1/2\pi\tau$) of 16.4 GHz. The IBM process SiGe BiCMOS 5HPE is available through MOSIS and features 40 GHz NPN bipolar transistors along with 0.35 μm CMOS.

Progress Report

Last year as we prepared to submit a chip with test circuits and a partial ADC circuit we found that IBM had changed the availability of our chosen IC fabrication process (IBM 6HP SiGe BiCMOS), making it unaffordable for us, at roughly 3 times the previous price. This prompted us to change our design to the IBM 5HPE process, with 0.35 μm features rather than the 0.25 μm of the 6HP.

Unfortunately, changing processes is not a trivial matter. Our design uses enclosed layout transistors with guard rings for radiation hardness, which are not a standard IBM part. On our last chip design project we were able to use component libraries and Cadence rules files developed at LBNL, CERN, and Rutherford, but these libraries are not available for the BiCMOS process we have chosen for this ADC. We have implemented parameterized cells (PCELLs) for the transistors (radiation-hard circular gate MOSFET's) and re-written the Cadence rules files to enable them to be laid out and extracted. We also had to change the sizes of all transistors in all circuits to suit the larger feature size of the new process and do some redesign to accommodate the larger feature sizes.

A major difficulty we encountered in the redesign is that the amplifier used in the sample-and-hold circuit designed in the 6HP process is not fast enough in the 5HPE process. We spent significant effort designing a faster amplifier in the new process.

We currently have a layout in the 5HPE process for a chip containing all the elements for a 3-bit block of the ADC shown in Fig. 2. The required bias generators to run the chip has also been designed. A picture of the chip is shown in Fig. 3. Many internal points are brought out to pads so we can test the circuits individually. For example, the output of the sample-and-hold is brought out as are the seven comparator outputs. In simulations from the schematic and from extracted layouts, the comparators and the decoder circuit are all fast enough to run at the desired clock frequency (714 MHz = 1/1.4 ns), but more refinement of the amplifier is still needed.

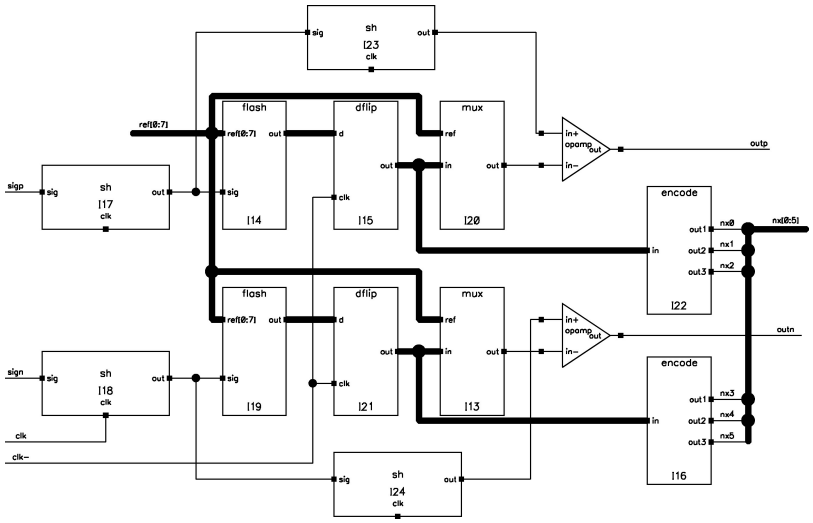

Figure 2. Schematic of a 3-bit cell.

Our plan is to submit the chip for fabrication in August, 2007. We will continue to improve the design while waiting for the chip to be delivered and then test the fabricated chips. For FY08, we will irradiate the chip to test the radiation hardness and refine the design based from the results from the first prototype chip and submit one more prototype.

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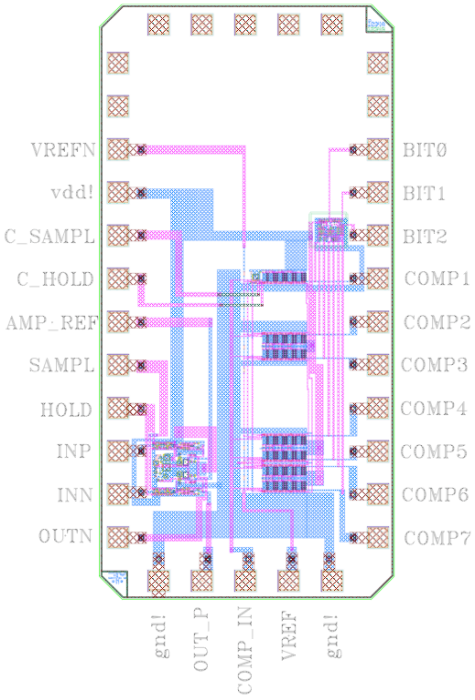

Figure 3. Picture of a 3-bit cell.

Budget Description

The design work is performed by an electrical engineer with the help of a technician. The technician has a Bachelor degree in electronic engineering technology from DeVry University and is currently studying part time for a Bachelor degree in electrical engineering at The Ohio State University. He has worked on the optical electronics for the pixel detector of the ATLAS experiment over the last few years. The MOSIS cost for the prototype digitizer using the IBM 0.35 Micron SiGe BiCMOS 5HPE process is $27,000.

Budget

Inst.	Item	FY03	FY04	FY05	FY06	FY07	FY08
OSU	Other Professionals (Technician/Engineer)	20,232	20,232	20,603	18,434	21,051	21,051
OSU	Fringe Benefits	5,463	5,463	5,563	4,977	5,705	5,705
OSU	Total	25,695	25,695	26,616	23,411	26,756	26,756
OSU	Travel	1,259	1,259	1,259	0	0	0
OSU	Digitizer	0	20,000	34,000	0	0	0
OSU	Indirect costs	13,046	13,046	13,575	11,589	13,244	13,244
SLAC		0	0	0	0	0	0
	Grand total	$40,000	$60,000	$75,000	$35,000	$40,000	$40,000

* Indirect cost is 49.5% for personnel and travel.

Bibliography

1. Marc Ross, private communication.

2. www.cadence.com

3. K.K. Gan *et al*., "Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector", Nucl. Phys. B (Proc. Suppl.) 125, 282 (2003).