An Upgrade for the Beam Position Monitoring System at the Cornell Electron Storage Ring*

M. Palmer†, J. Dobbins, D. Hartill, C. Strohman, Cornell University, Ithaca, NY 14853, USA

Abstract

We describe the design and initial characterization of a fast (nanosecond time scale), high resolution (micron level) beam position monitoring system for use in the Cornell Electron Storage Ring (CESR). Beam position monitoring requirements at CESR include 1) precision orbit measurements in the interaction region and near the synchrotron x-ray beam lines, 2) monitoring of individual bunch positions during multi-bunch high energy physics (HEP) operation, 3) single pass measurements to monitor injected bunch oscillations and injection transients, and 4) operation at both HEP and injection current levels which vary by 5 orders of magnitude. The ready availability of electronic components with large bandwidth and dynamic range for the communications industry has allowed us to economically implement a system providing this range of capabilities.

1 INTRODUCTION

The Cornell Electron Storage Ring (CESR) provides colliding beams for high energy physics (HEP) research by the CLEO collaboration as well as synchrotron light to multiple beam lines for use by Cornell High Energy Synchrotron Source (CHESS). Detailed orbit measurements are critical to providing acceptable machine performance for both of these applications. Unfortunately, the present CESR beam position monitor (BPM) readout system is not suitable for continuous operation during HEP running [1]. Thus we have undertaken the design of a BPM readout system for continuous use in multi-bunch CESR operation.

Several additional issues have been identified which a new design should address. High precision measurements, at the micron level, can aid in studies of CLEO solenoid compensation for luminosity performance and also improve our ability to control the orbit near the CHESS beam lines. Overall CESR performance is strongly coupled to our injection efficiency [2]. Improving our capability to monitor injected bunch oscillations and injection transients is expected to significantly aid our efforts to improve injection. This imposes the requirements that a new system be able to operate at sub-microamp bunch currents and to make single-pass measurements of particular bunches.

2 BPM READOUT DESIGN

In order to satisfy the design criteria described above, a wide-band readout system has been designed that provides simultaneous readout of all 4 buttons in a CESR beam position detector. Figure 1 shows the major components of the new design. There are 3 primary boards per module: an *analog board* holding the front end and analog-to-digital converter (ADC) for each button; a *timing board* referenced to CESR's precision timing system clock [3] which provides overall module timing control in steps of 20 ps as well as relative beam button delay adjustments of the same size; and a *digital board* that controls operation of the module, handles communications with the CESR control system, and provides a digital signal processor (DSP) for on-board data processing.

* Work supported by the National Science Foundation

† palmer@mail.lns.cornell.edu

2.1 Front-End Electronics

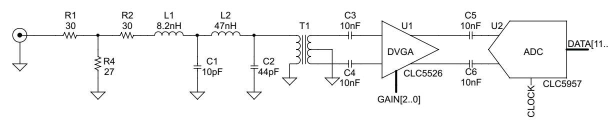

Figure 2: Design of the front-end filter along with the DVGA and ADC stages for a single button.

Figure 2 shows the front-end electronics design used for each beam button. It consists of 3 sections. The first is a discrete filter network to restrict the bulk of the signal to the 300 MHz bandwidth of the National CLC5526 digital variable gain amplifier (DVGA). The DVGA supplies a gain range of -12 to 30 dB in accurate steps of 6 dB, thus meeting our dynamic range requirements. The third section is a 12-bit, 70 MSPS (300 MHz input bandwidth) CLC5957 ADC, also from National.

Figure 3 shows the simulated response of the front-end filter to a typical beam button signal in CESR along with a recent measurement of the actual digitized output. The two curves are in reasonable agreement, thereby validating the basic performance of our design.

The use of separate readout chains for each of the four beam buttons requires that the individual gains be well matched to avoid significant errors in measuring the electrical center of the set. To first order, displacements from the center of the beampipe can be written as:

$$x = x_0 \left(\frac{S_1 + S_2 - S_3 - S_4}{S_1 + S_2 + S_3 + S_4} \right), \qquad (1)$$

where the S_i are individual button signals and x_0 is a scale length. If the S_i are subject to a fractional gain error, δ, then we expect x to vary by $x_\epsilon \sim x_0\,(\delta/2)$. For our front ends, the DVGA and ADC outputs are good to 1% over their operating range and we estimate the errors associated with the filter network to be a few percent. Thus we assign $\delta \leq 0.05$ as the worst case. The majority of CESR BPMs have $20 \leq x_0 \leq 28$ mm corresponding to $x_\epsilon \leq$ 0.5-0.7 mm, a level we deem acceptable.

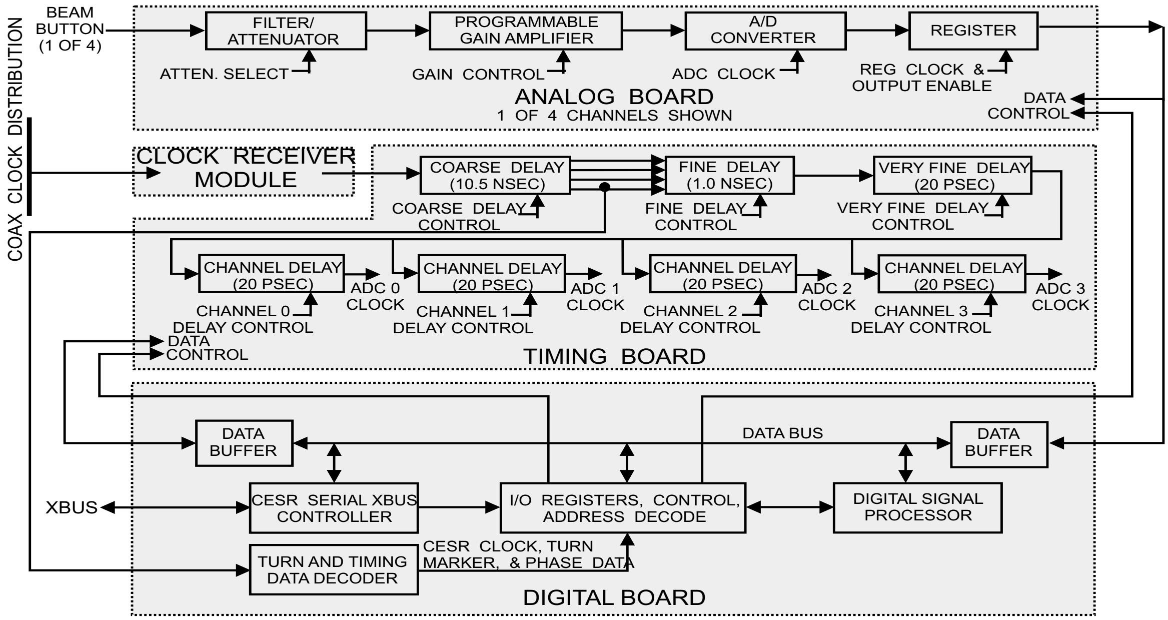

Figure 1: BPM Readout Module Block Diagram

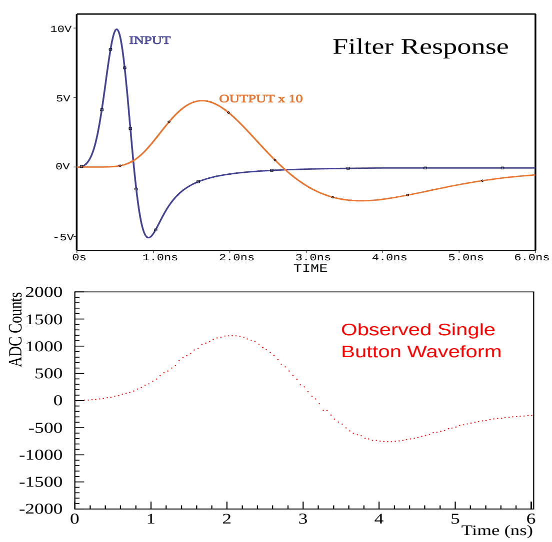

Figure 3: The top plot shows our simulation of the expected response of the front-end filter to a typical button signal. The bottom plot shows the observed response of a beam button in CESR. To create this plot, a timing scan was taken and 32 readout samples were collected at each point.

2.2 *Timing Electronics*

Figure 4 shows the timing control circuit which allows adjustment of the module timing relative to the CESR timing system clock with 20 ps granularity. The use of phase-locked loop clock generators for the 10.5 ns (AMCC4402) and 1.0 ns (CY7B991) timing steps minimizes timing jitter in the readout. 20 ps adjustments for the overall module timing and for relative timing of individual buttons are provided by a PECL programmable delay chip (MC100E195).

The relative adjustments will allow us to keep all button samples within a ± 10 ps window. For the output waveforms as shown in Figure 3, 10 ps corresponds to approximately 0.03% variation in the peak signal on a particular button. Using Eqn 1, this implies absolute errors of 6–8 μm due to the relative timing of the button readout. If more precision is required (*eg.*, when comparing trajectories of different bunches), the overall module timing can be scanned through the top of the signal peak and the resulting data fitted to obtain the best estimate of the peak signal.

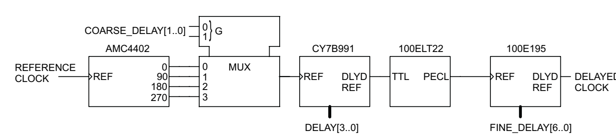

Figure 4: Design of the overall timing control circuit for each module. Phase-locked loop clock generators provide 10.5 ns and 1.0 ns timing adjustments while a programmable delay chip provides 20 ps adjustments.

2.3 *On-board Signal Processing*

Significant on-board processing capability is provided by an Analog Devices SHARC DSP. This capability is key to our plan for the final operational system. It allows each module to automatically determine peak position for each beam button as well as set the appropriate gain for making measurements of a particular bunch. It also provides the processing capability necessary for making betatron phase and coupling measurements which are a key diagnostic for maintaining CESR performance [4]. We are currently in the process of implementing the DSP code which is required for this level of capability.

3 PRELIMINARY SYSTEM TESTS

We have conducted a number of tests using prototype readout modules that provide essentially all of the functionality of the final design except for having no local DSP. This has let us characterize the performance of the front-end and evaluate the system's potential. Figure 5 shows a timing scan over a period that allows us to see one train each of electrons and positrons pass the BPM. The system readily resolves individual bunches except for those that have a nearby parasitic crossing point. Figure 6 shows the performance at low currents in CESR. Single pass measurements with microamp currents are possible. Finally, Figure 7 shows the vertical position measurement obtained from a series of 2048 samples acquired on successive turns. This implies that we can achieve 1μm resolution by integrating over as few as a thousand turns in CESR.

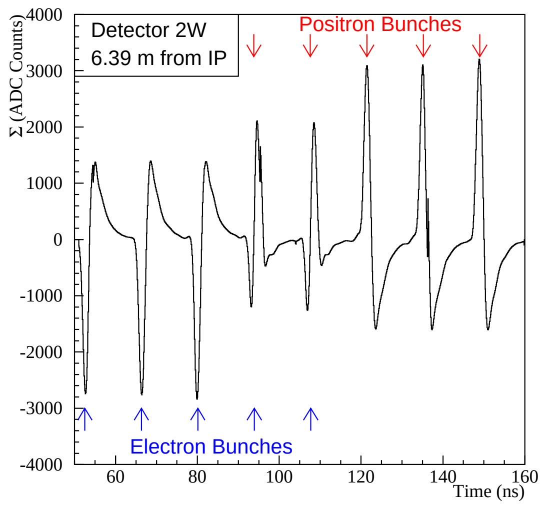

Figure 5: Timing scan for a detector located 6.39 m from the CLEO interaction point taken during HEP conditions. The new readout cleanly resolves the CESR bunch structure. Note that signals from the last two electron bunches and first two positron bunches are overlapping due to the proximity of this detector to their parasitic crossing point.

4 CONCLUSIONS

We have successfully tested the prototype for a new BPM readout system for CESR. Work continues to implement the full range of capability of the new system. In particular, automated calibration and timing capability is being developed for the DSP to allow efficient autonomous readout of each detector. The first 15 modules are slated to be installed around the CESR ring later this summer.

5 ACKNOWLEDGEMENTS

We would like to thank Mike Billing, Stuart Henderson, Raphael Littauer, Bob Meller, John Sikora, Gerry Codner and John Barley for their helpful discussions over the course of this project.

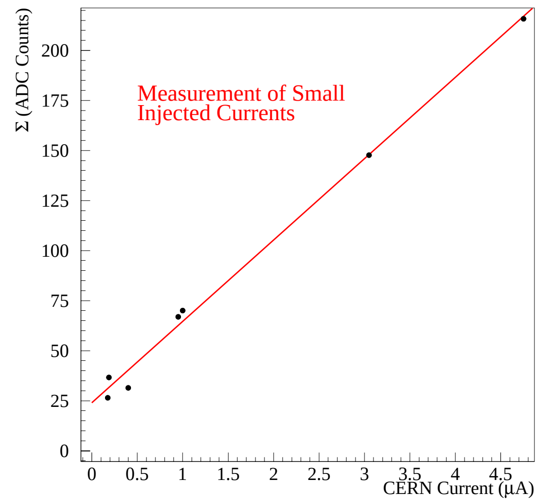

Figure 6: The current signal obtained with a prototype module versus our our CERN Current Monitor value.

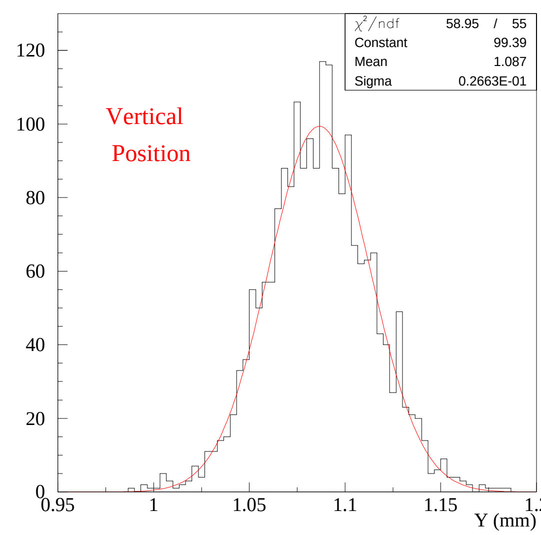

Figure 7: The distribution of vertical position measurements obtained from 2048 samples taken on consecutive turns. The single-pass resolution is approximately 27μm.

6 REFERENCES

[1] The present CESR BPM readout system is relay-based where a single readout circuit is used to read each button on a detector in sequence. This prevents single pass orbit measurements. The finite lifespan of the relays also prevents high duty cycle operation during HEP conditions.

[2] Stuart Henderson *etal.*, "Improvements to the CESR Injector and Injection Process", RPPH117 this proceedings.

[3] Robert E. Meller, "Precision Timing Control System", Proc. of the 1997 IEEE Particle Accelerator Conference, p2505.

[4] D. Sagan *etal.*, Phys. Rev. ST Accel. Beams **3** 092801 (2000).