

SLAC-LLNL ILC Damping Ring Kicker High Availability Modulator R&D Program

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Craig Burkhart

for the SLAC-LLNL Team:

E. Cook (LLNL)

A. Krasnykh, R. Larsen, T. Tang (SLAC)

Overview

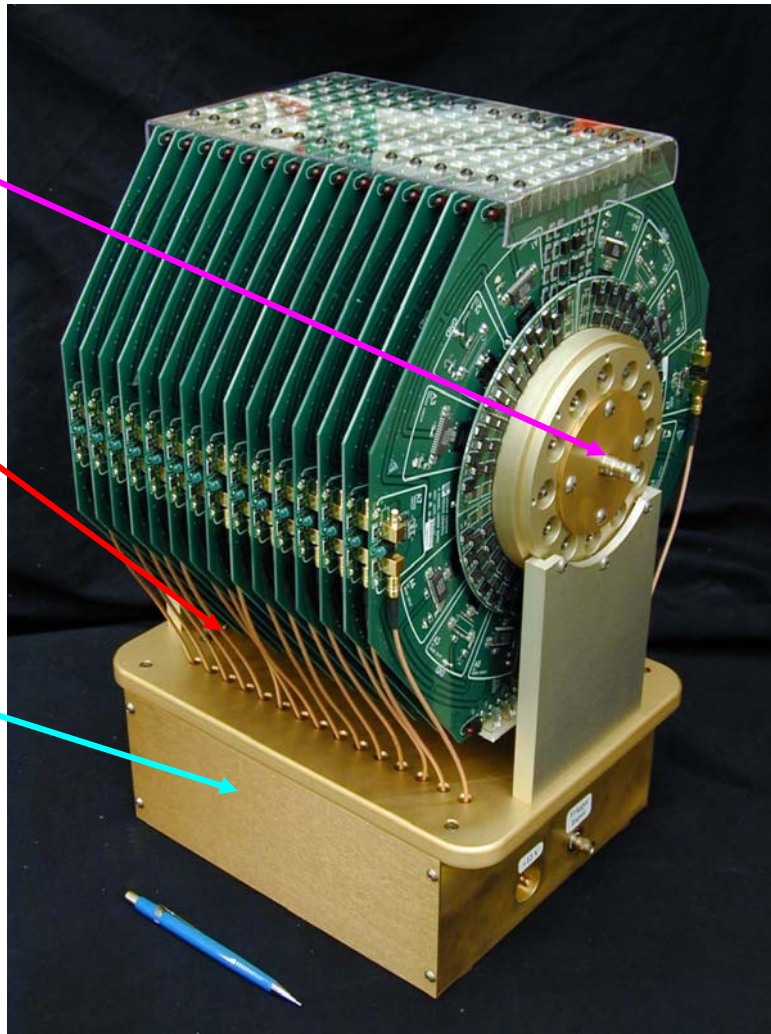
- SLAC-LLNL program is investigating two approaches
 - Inductive adder topologies
 - DSRD (opening switch) topologies
- FY07 results and present program status
- FY08 Plans

ATF Kicker Modulator

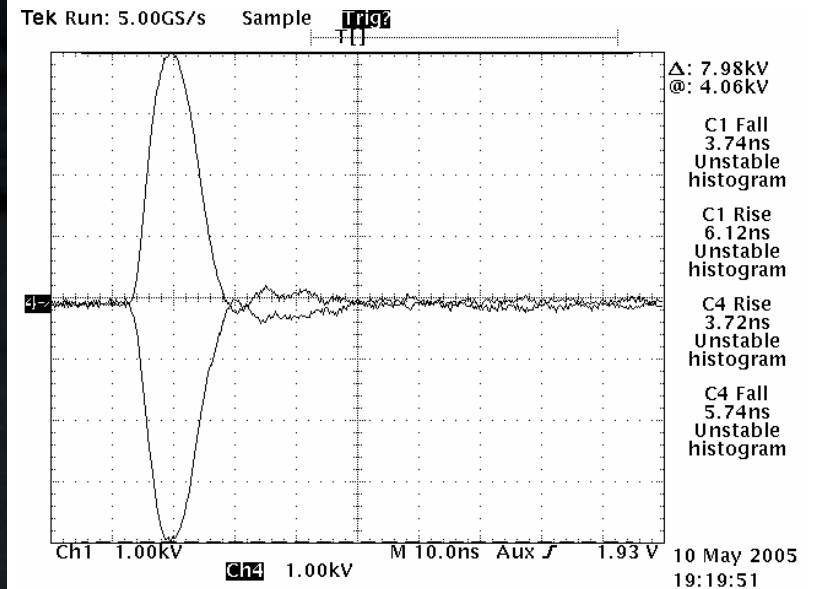
Output connector

Trigger Cables

Houses trigger distribution, power supplies, etc

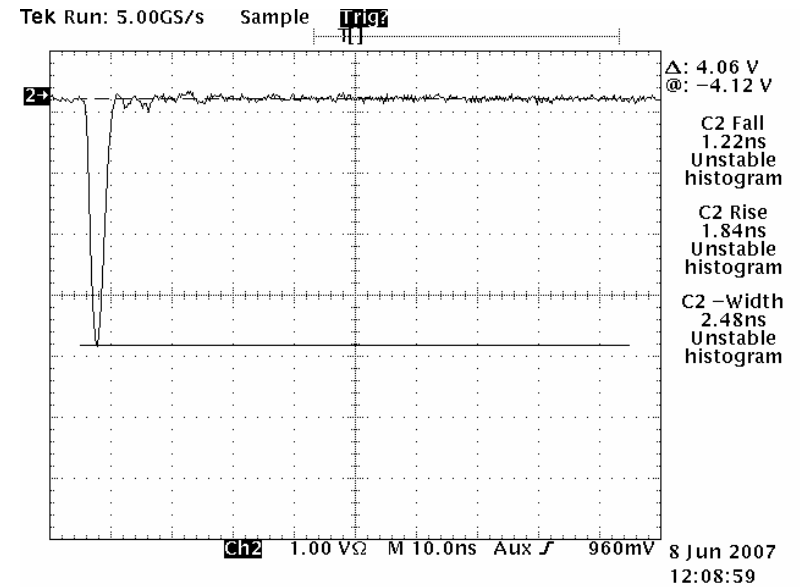
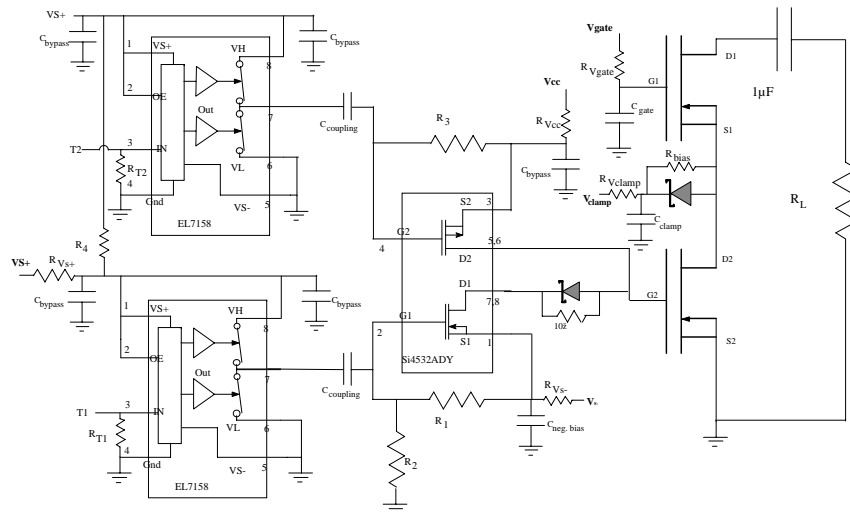


Positive and negative polarity pulses. Measurements made with two identical high voltage probes



Courtesy of E. Cook

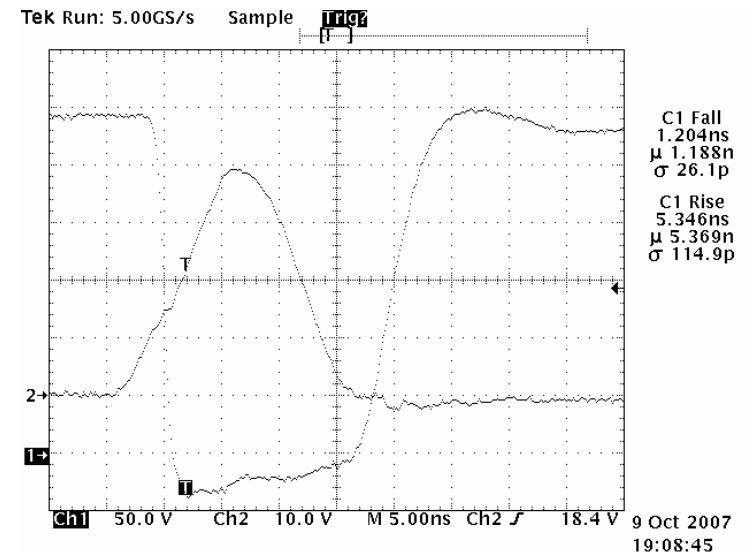
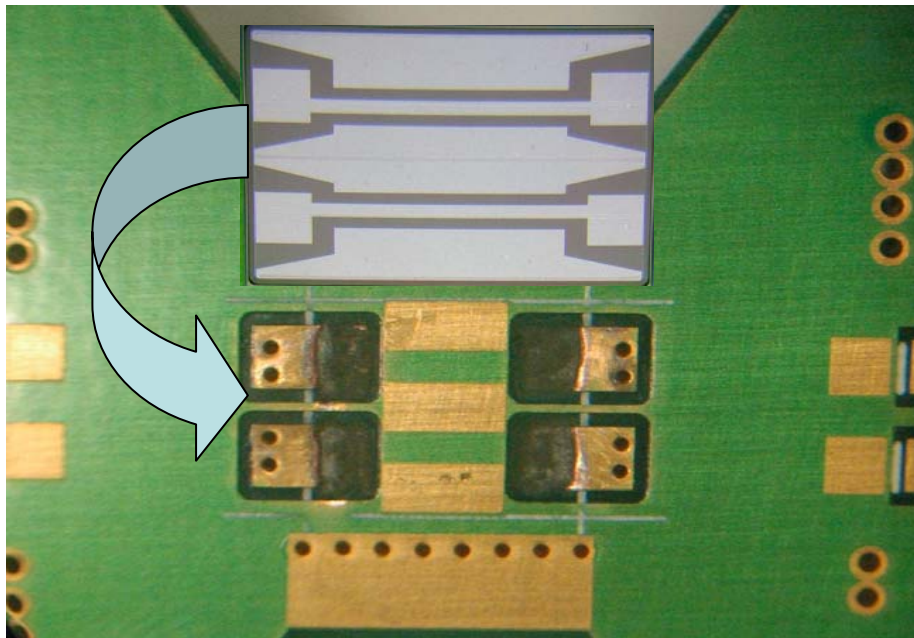
Ultra-fast Switch R&D: Cascode



- Reduced loading on driver circuit
- Lower impedance output stage drive
- Higher driver voltage
- Short pulse duration: 2.5 ns FWHM
- Fast rise/fall time: <2 ns
- Challenge: controlling output voltage

Data courtesy of E. Cook

Ultra-fast Switch R&D: Hybrid

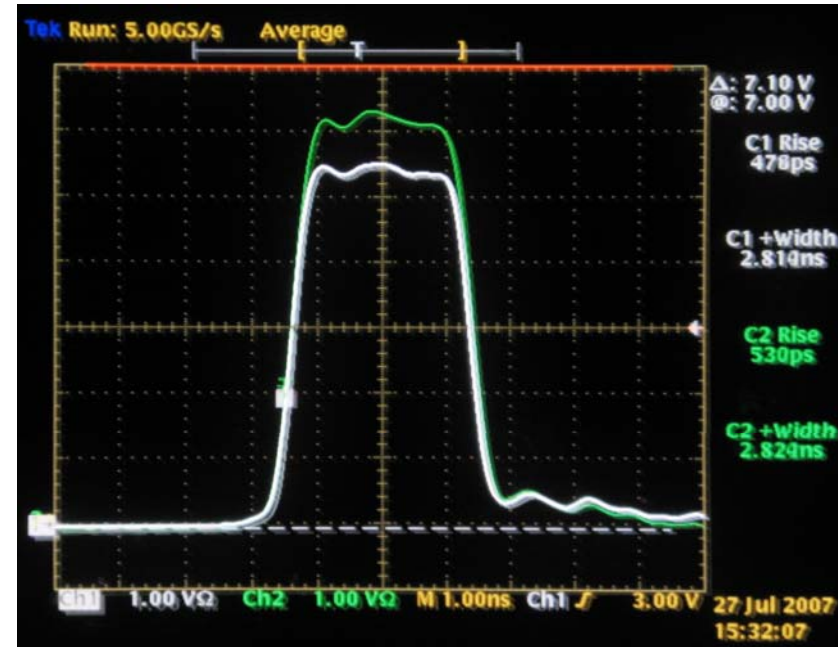


- Die-form driver & FET
- Eliminate package inductance
 - Better control of gate charge
 - Reduce source $L di/dt$ voltage

- Fast output risetime: 1.2 ns (Ch1)
- Excellent gate control (Ch2)
 - High output voltage
 - Low R_{DS-on}
 - $V_D = 400$ V
 - Driver not optimized for short pulse

Data courtesy of T. Tang

Ultra-fast HV Diagnostic R&D

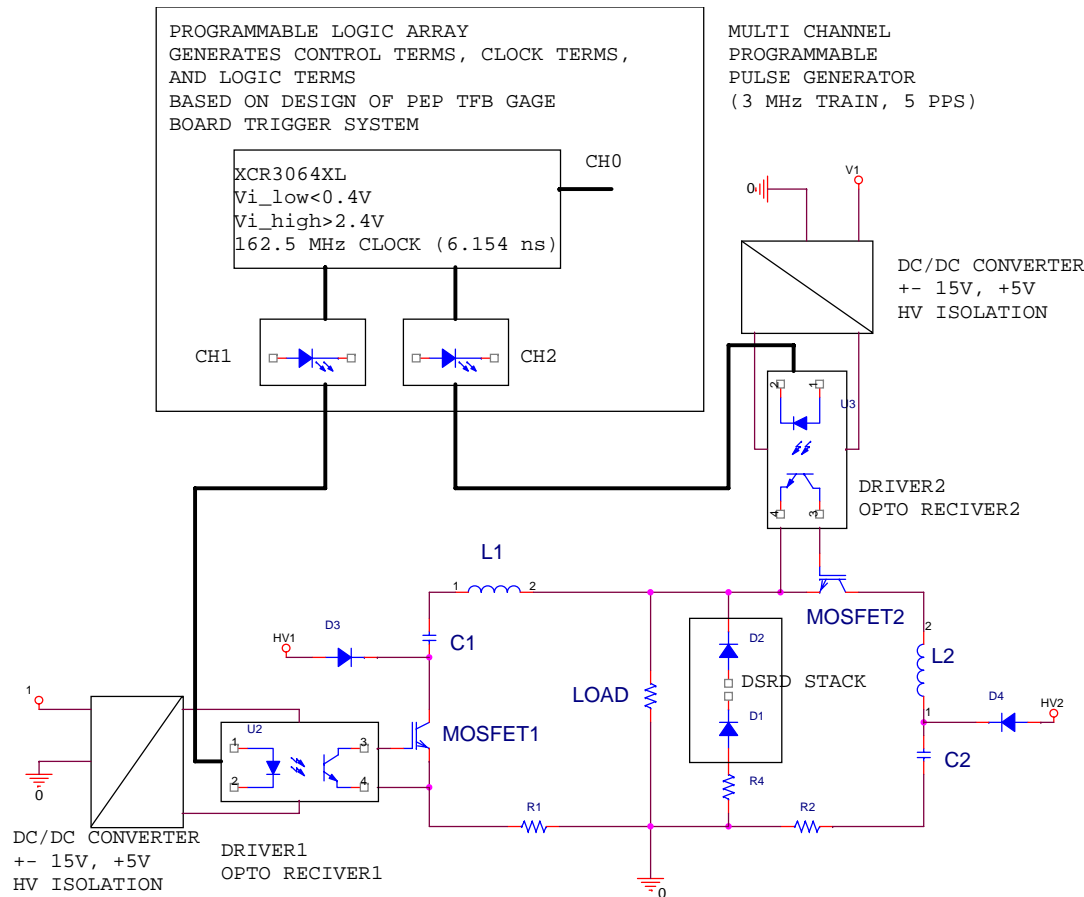


- Prototype broadband power divider
- Compact, 2nd generation version under construction, using tested SMD resistors

- Comparison with commercial, low power, low voltage, high bandwidth divider

Data courtesy of A. Krasnykh

DSRD Diagnostic Test Stand



- Characterize DSRD to 6 kV
- Independent forward and reverse drive

Data courtesy of A. Krasnykh

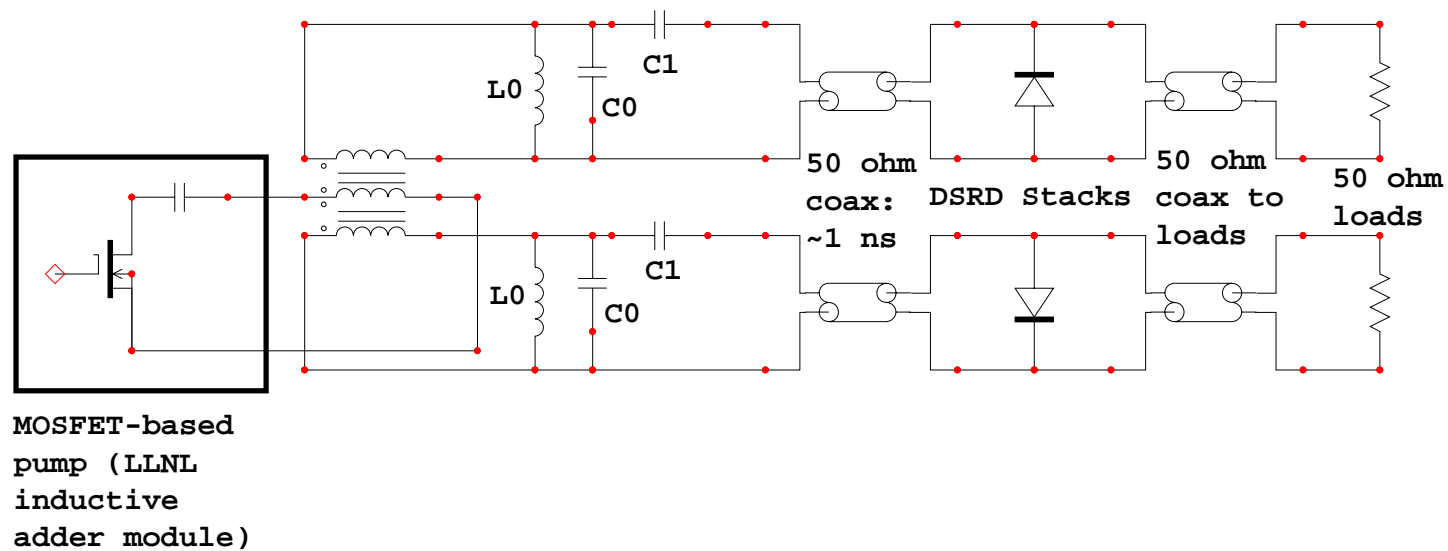
FY08 Inductive Adder Program

- 2nd generation hybrid driver/FET circuit
- Module development; parallel arrays
 - Cascode
 - Hybrid
- Adder structures
 - Conventional adder structure cannot meet 3 ns bunch spacing requirements; transit time >1 ns
 - Investigate “compact” structures, e.g. transmission line transformer
- “Scale” modulators
 - Identify bandwidth limitations of module and adder cell approaches

FY08 DSRD Program

- Develop prototype DSRD kicker modulator
 - ± 5 kV into 50Ω
 - Flattop ~ 2 ns, rise/fall ~ 1 ns (fundamental limit for 500 V p-n Si junction)
 - PRF thermally limited (DSRDs from Ioffe, no thermal management structure, DTI has USDOE SBIR funding to work with VMI to commercialize DSRD with heat sinks)
 - Deliver to KEK for testing on ATF2

Prototype Schematic



Summary

- FY07 Results
 - Modest progress (funding limitations)
 - Ultra-fast FET switching
 - High bandwidth HV diagnostics
 - DSRD test stand
- FY08 Program
 - “Scaled” inductive adder assemblies
 - Prototype DSRD modulator
 - Funding cuts may limit progress