R&D on the fast injection/extraction kickers

- *DSRD-based ILC DR Kicker Activity at SLAC*

- *ILC DR Pulser Activity at DTI*
  (under DoE SBIR grant DE-FG02-06ER84459)

The R&D team: *Floyd Arntz (DTI, Bedford, MA)*

Alexei Kardo-Sysoev (DTI consultant)

Dennis Kemp (VMI, Visalia, CA)

Anatoly Krasnykh (SLAC and DTI consultant)

DSRD based ILC DR Kicker Activity at SLAC

- HV Broadband Coupler
- HV Subnanosecond Range Power Dividers
- HV DSRD Diagnostic Stand

Even do not think to use these!

HIGH VOLTAGE PULSE ATTENUATOR

MODEL 2237-HFNFP, 2239-HFNFP

Model 2239 HFNFP

Model 2237-HFNFP

DESCRIPTION:
26dB attenuators with
HN female input connectors.

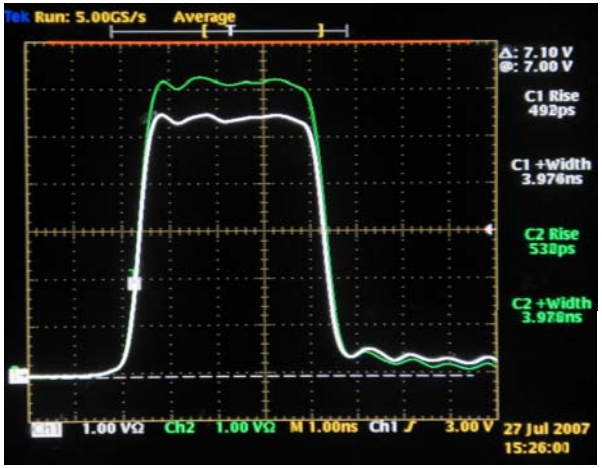
50 Ohm Input Impedance

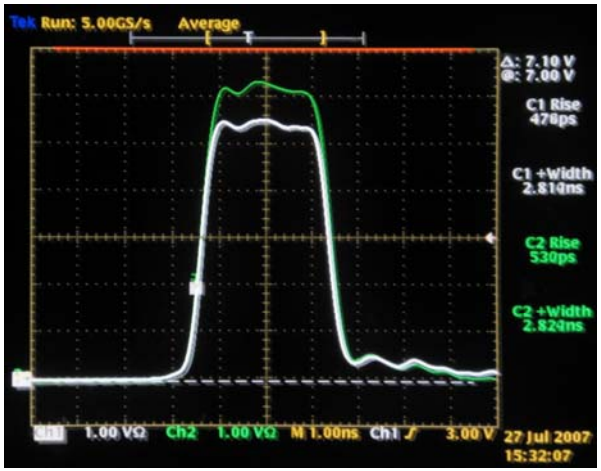
$5325 ea

Model 142-xxx-yy

$3009 ea

DSRD based ILC DR Kicker Activity at SLAC (cont.)





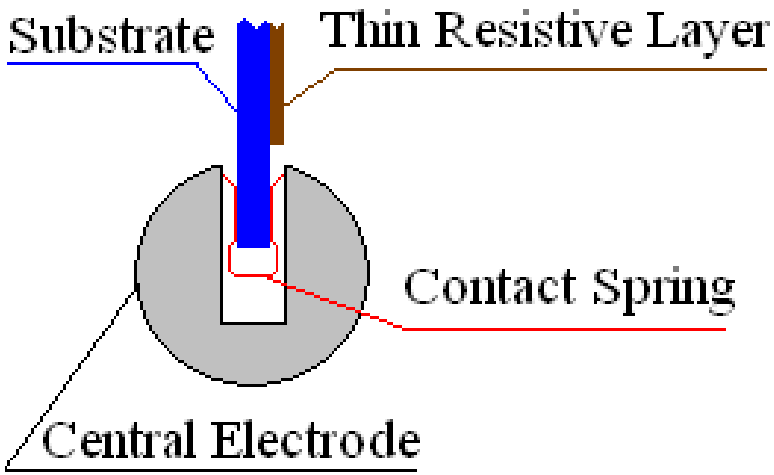
Home made HV Pulse Power Dividers

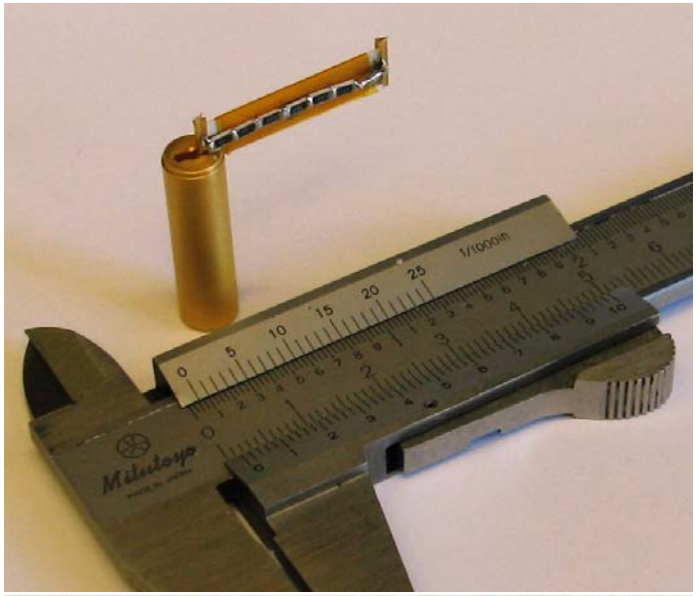
DSRD based ILC DR Kicker Activity at SLAC (cont.)

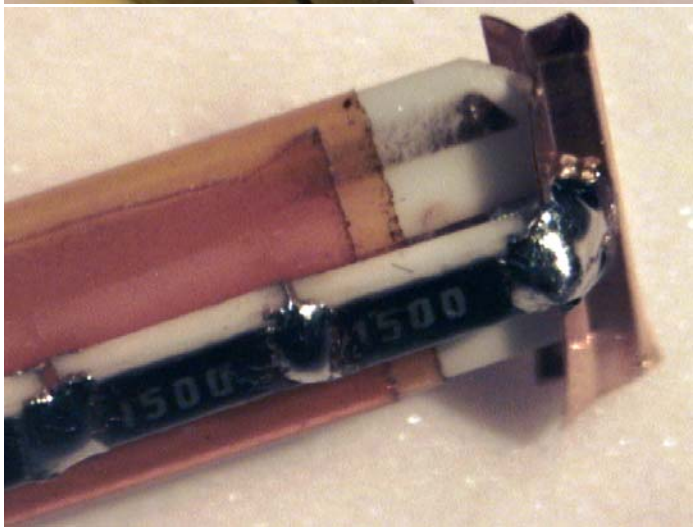
Prototype PD03

Technological Idea of Realization

(know how)

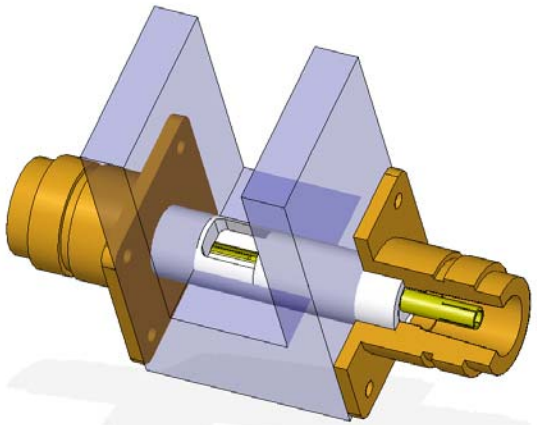




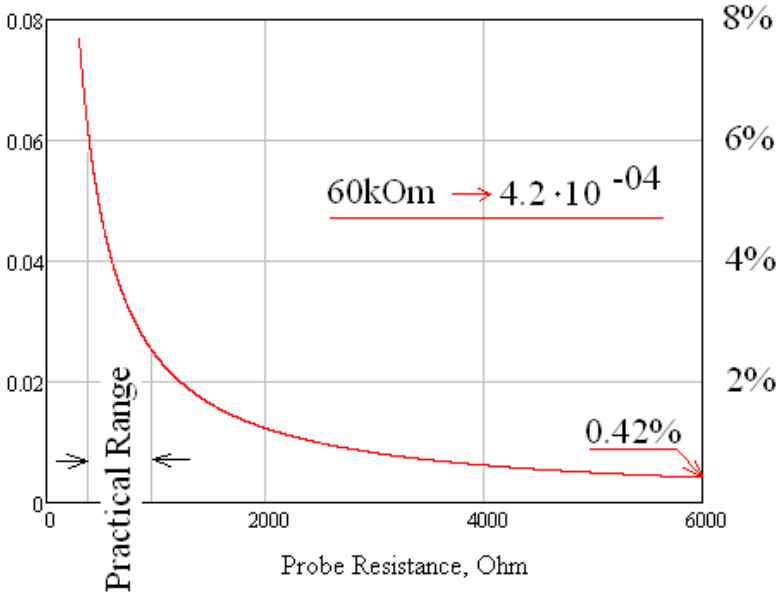


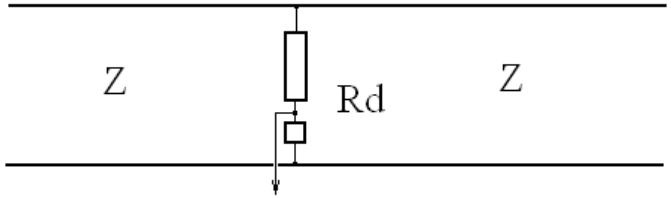
- 1203 case of SM Resistors Array (prototype)
- Flexible joint vs. temperature variation
- (2-3) W dissipation through ceramic substrate
- Sharp edges of contact spring are inside central electrode of coax

DSRD based ILC DR Kicker Activity at SLAC (cont.)



Home Made HV Power Dividers



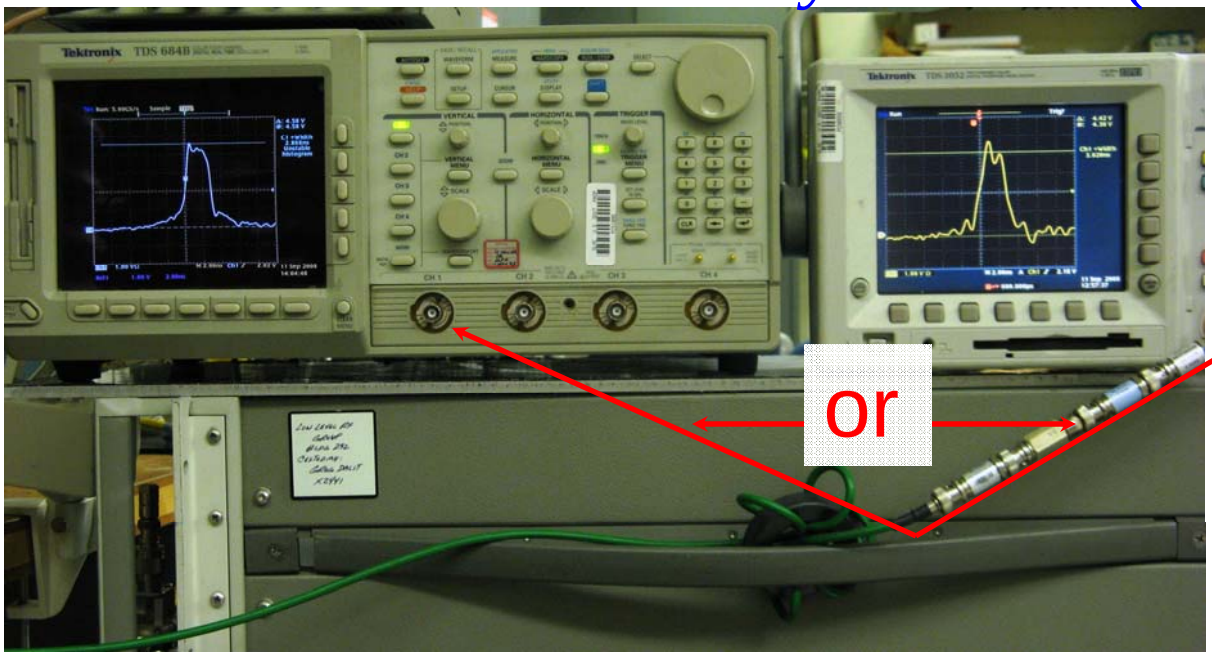


HM PDs and couplers will not meet the residual energy spec.

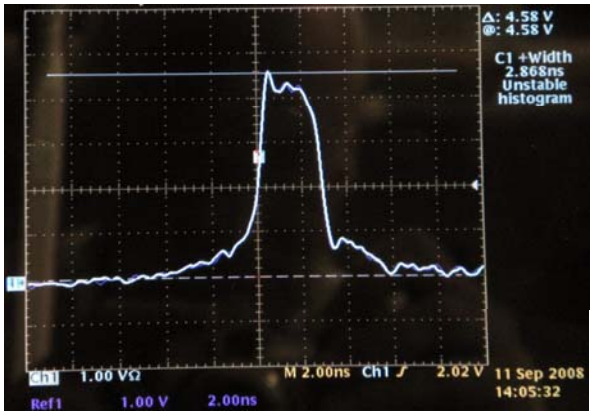
The spec on the residual energy between pulses will require SWR=1.0004 for the main components

DSRD based ILC DR Kicker Activity at SLAC (cont.)

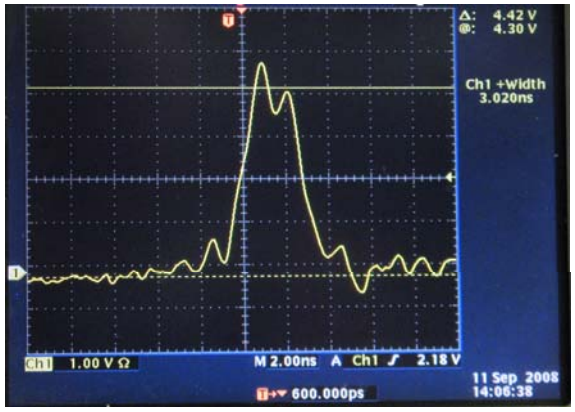
Diagnostic Tools



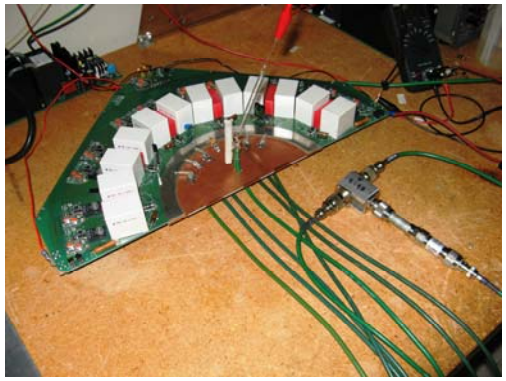
TDS 684B (5Gs/sec, BW=1GHz) *vs.* *TDS 3052 (5Gs/sec, BW= 0.5GHz)*

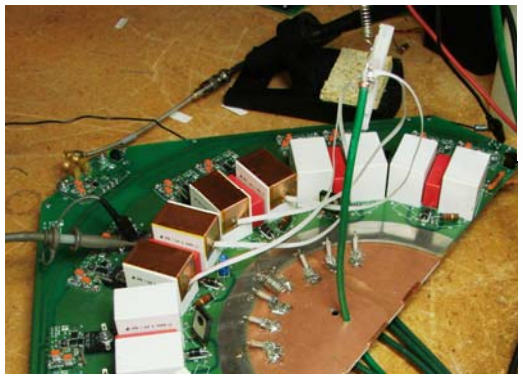


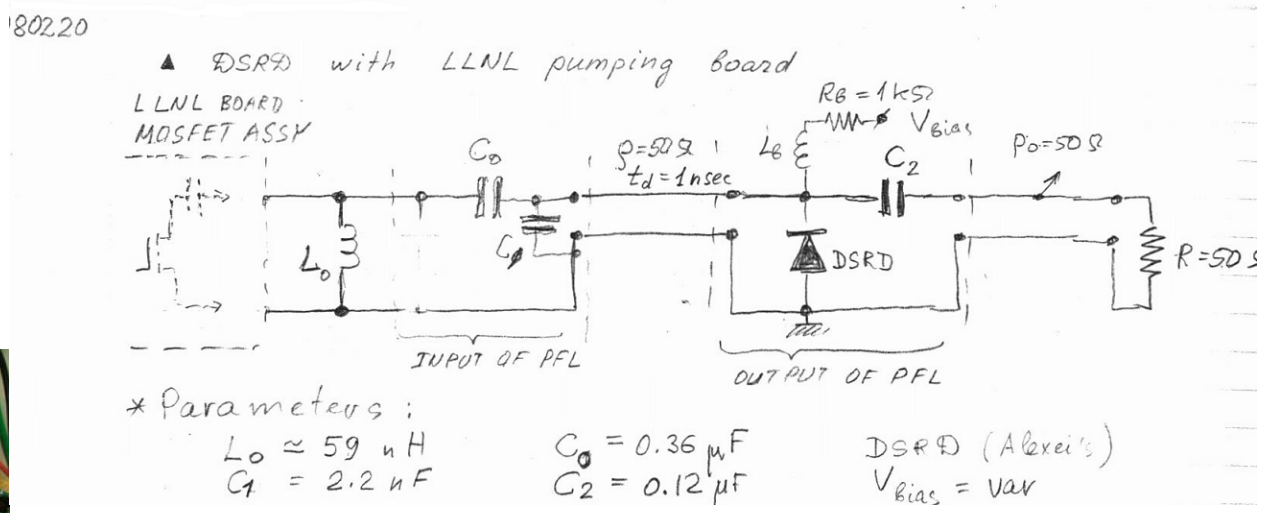
The cost, cost, …



DSRD based ILC DR Kicker Activity at SLAC (cont.)

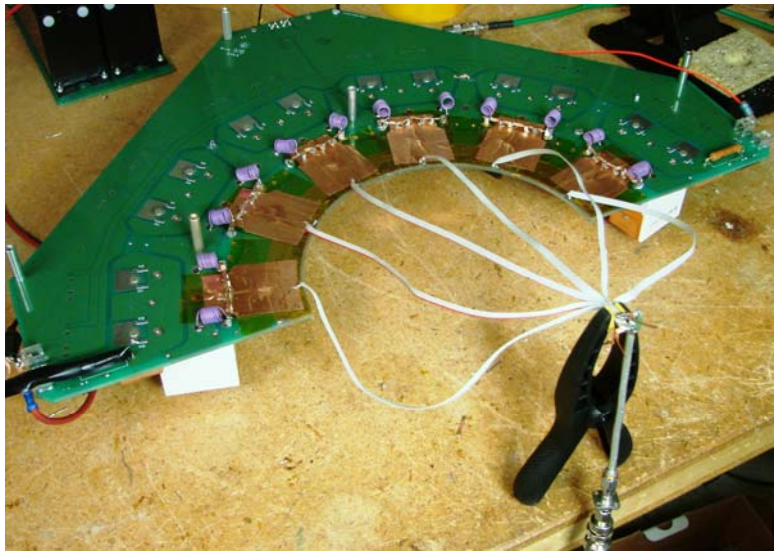


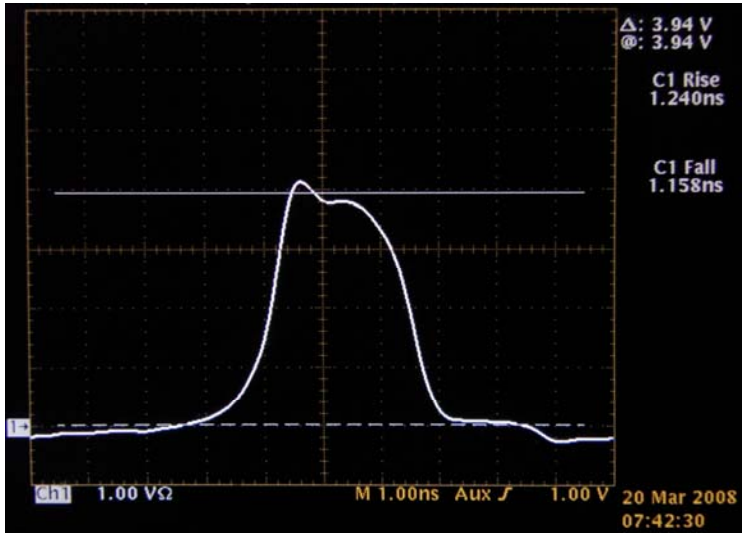


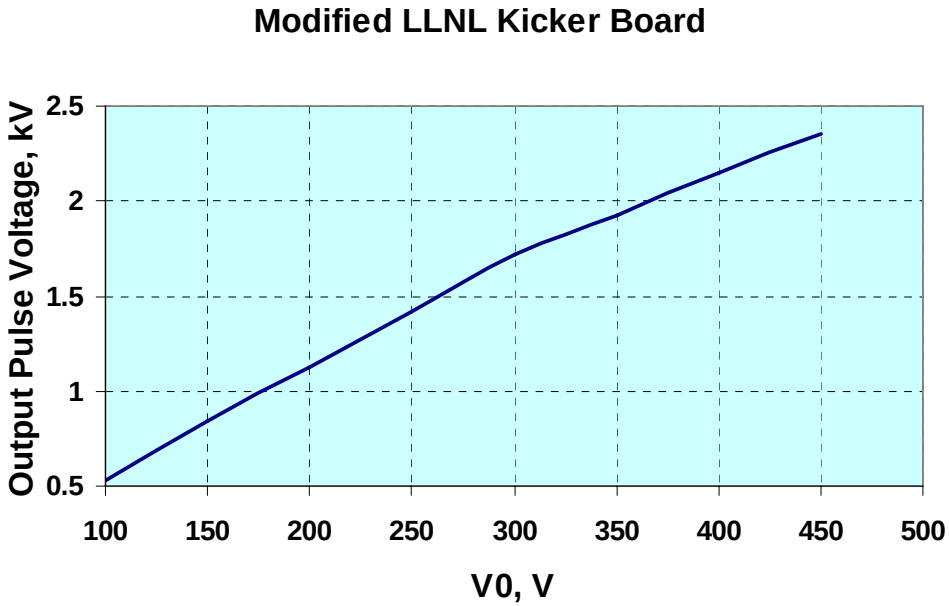


Develop of Low Gain DSRD Prototype Pulser Based on the LLNL Board Assembly

DSRD based ILC DR Kicker Activity at SLAC (cont.)





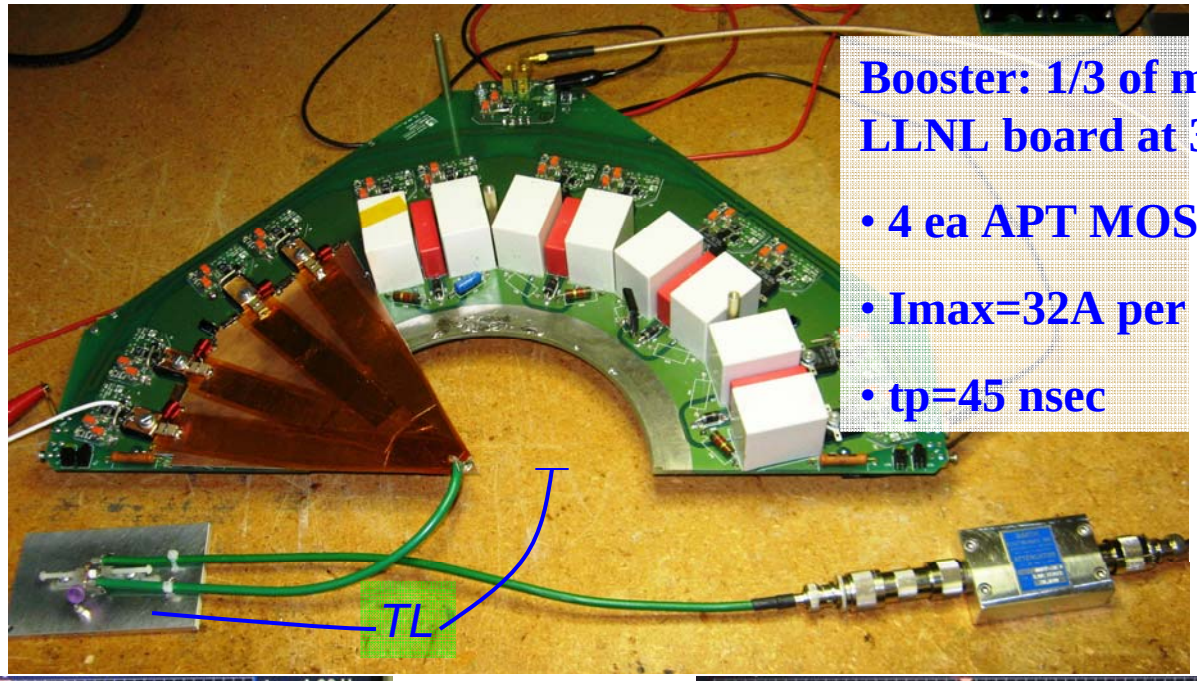


Main board components (capacitors, MOSFETs) are rather slow

Board was not designed for a high rep. rate

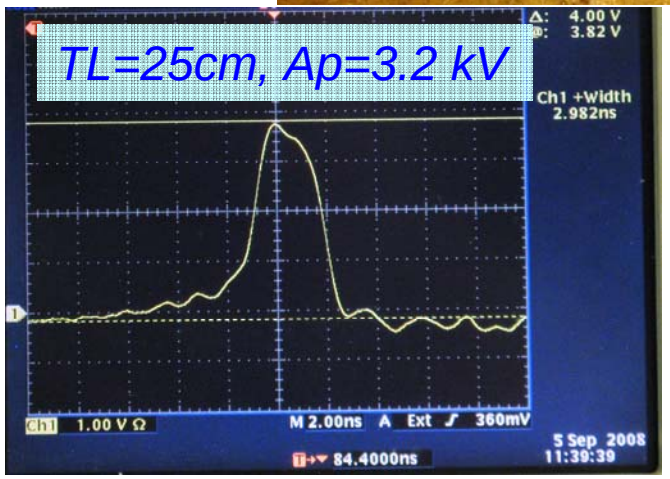
Experiments with the different board setups showed a PCB limitation for a realization of the DSRD method

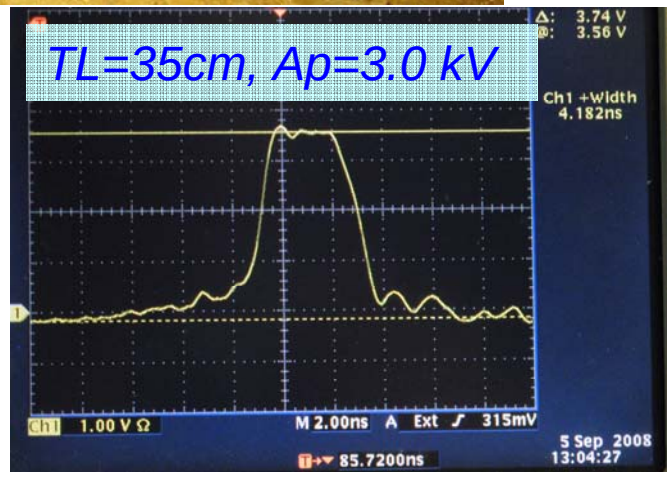
DSRD based ILC DR Kicker Activity at SLAC (cont.)



Booster: 1/3 of modified LLNL board at 300V

- **4 ea APT MOSFETs**
- **Imax=32A per MOSFET**
- **tp=45 nsec**





DSRD based ILC DR Kicker Activity at SLAC (cont.)

Problem:

How the “pre-pulse and after-pulse” i.e. the residual energy may be cut off

Short term plan

• optimization of tune (MOSFET voltages, number of cells vs. the DSRD voltage hold off and current density)

• Zener diode in series with the DSRD stack

(problem for a study: Zener diode thermal stability, reliability, package, etc.)

Long term plan (cost consuming!)

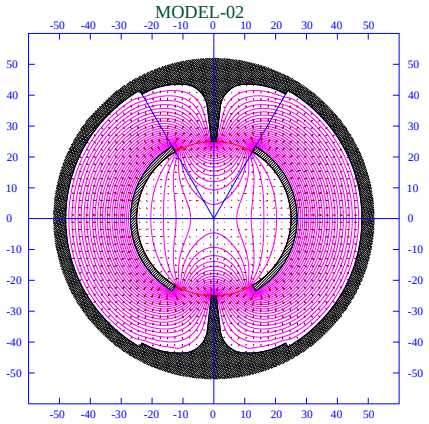
• Physical property of the DSRD for the ILC DR pulser (to optimize the doping and it profile, current density, package, etc.)

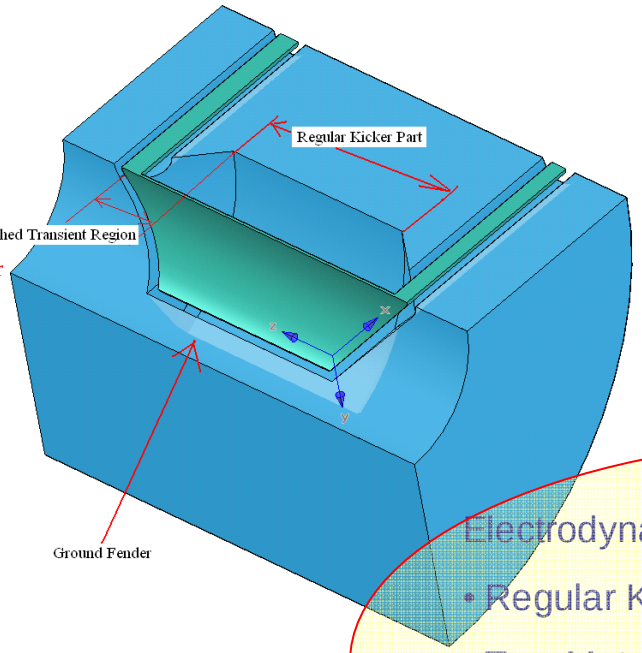
• see also Part II (*i.e. the Activity at DTI)*

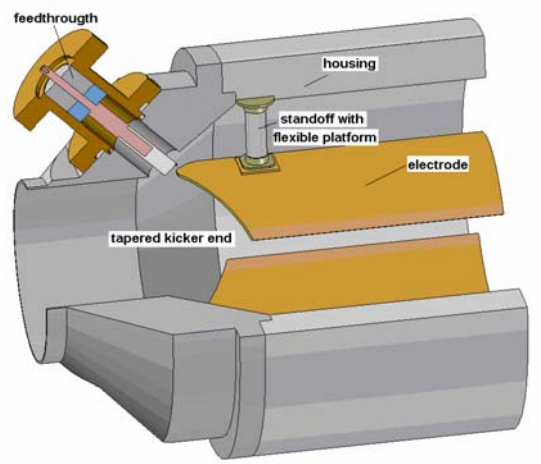
DSRD based ILC DR Kicker Activity at SLAC (cont.)

ILC DR Kicker Assembly (proposal)

Proposed Cross Section for the ILC DR Kicker







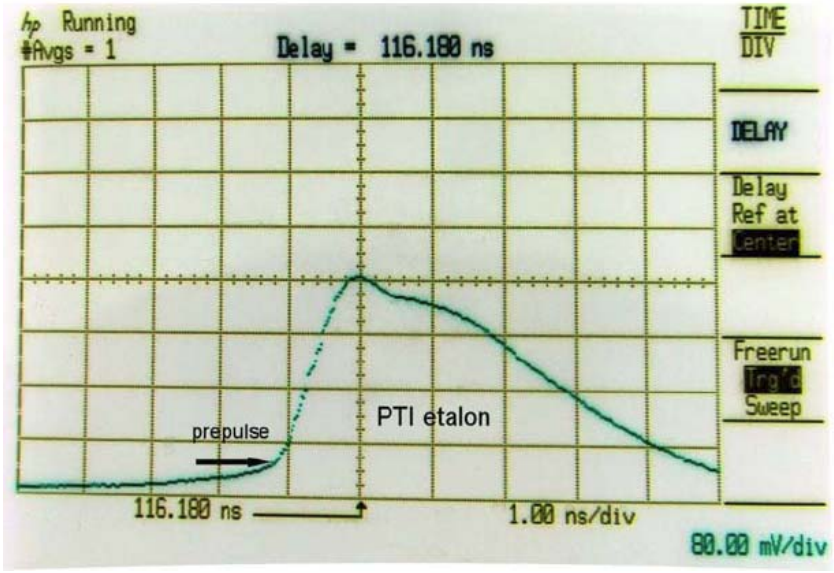
Quarter of Model is shown

Electrodynamic Structure with:

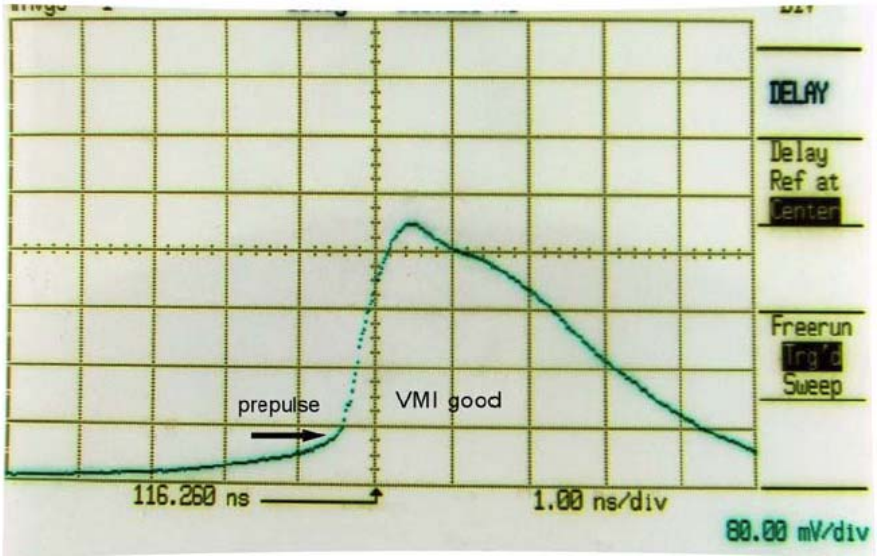
- Regular Kicker Part
- Two Matched Transition Regions at the Kicker Ends
- Ground Fenders
- Broadband Constant Impedance Feedthrough

ILC DR Pulser Activity at DTI

- *DSRD Technology Transfer to VMI*



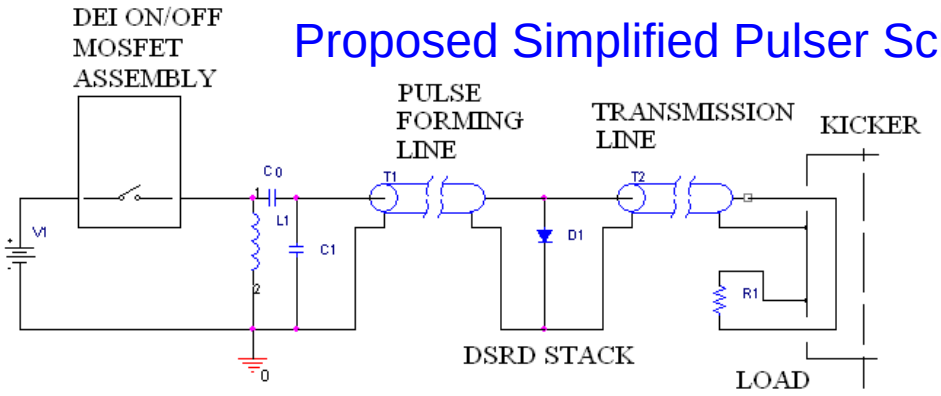
DSRD sample made in Russia



DSRD sample made by VMI

ILC DR Pulser Activity with DTI (cont.)

Proposed Simplified Pulser Scheme

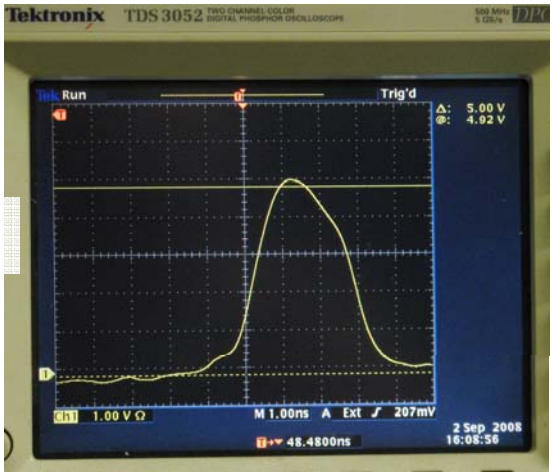


For details operation of the DSRD-based schemes see Part I of DRAFT at the FNAL site

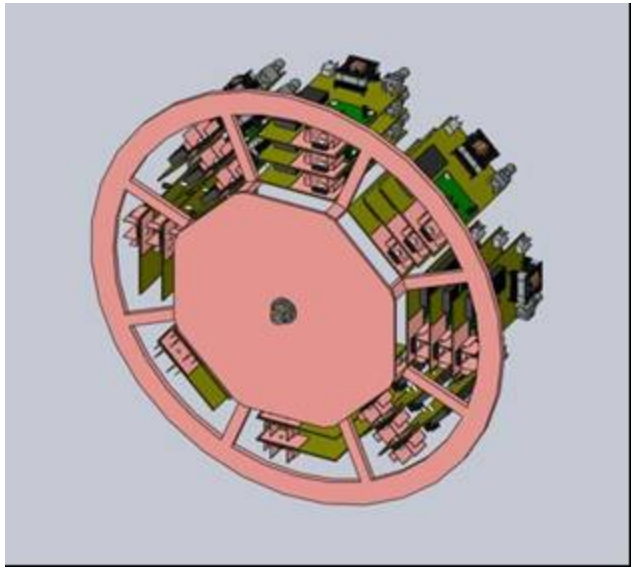
http://beamdocs.fnal.gov/AD-public/DocDB/ShowDocument?docid=3206

DSRD with PFL and TL

Two DE475-102N MOSFETs



ILC DR Pulser Activity with DTI (cont.)



Basic configuration of ILC DR pulser

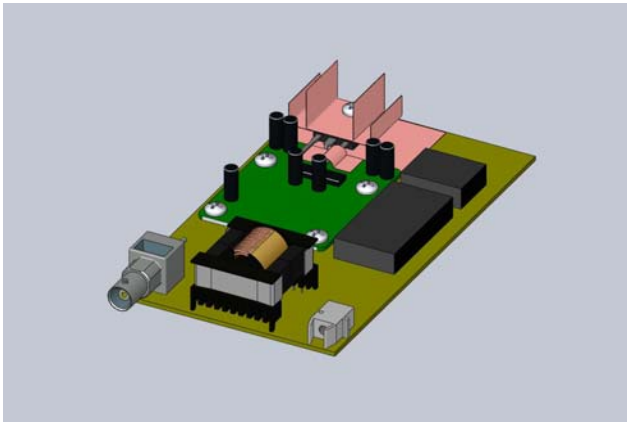


Illustration of individual MOSFET switching card. The pump system will employ eight parallel ranks of three (or four) of these in series. The series arrangement is required to withstand 2.5kV opening voltage.

ILC DR Pulser Activity with DTI (cont.)

• DTI has only worked with a hand-crafted breadboard HV MOSFET switch circuit for producing the 40-50 nsec pump pulses

• Presently DTI is working to finish the PC board design; and we regard the need for a second version as likely

• DTI plans on 3-high (series), 8-wide (parallel) array, each card capable of 25A. This should give a 200A total (peak) pump current and tolerate an opening voltage of 1600V

• DTI intends to operate ***only*** at 3MHz pulse rate ….but burst duration and bursts/second will be totally selectable. (The ability to adjust the latter parameters is needed for exploring DSRD thermal limits and the influence of thermal transients.)

• DTI ***does*** anticipate a need for tail biting (synchronous clamping) but will not introduce that until later. The same switch card design should serve this function

A rolling stone gathers no moss

and

Rome was not built in a day

The injection/extraction fast pulser technology based on the DSRD technology for ILC DR was not stopped due to the 2008 budget cut off. SLAC and DTI are continuing to work on this field.

The work at SLAC and DTI is conducted under SLAC/KEK collaboration and DoE SBIR grant accordingly. The progress is proportional to the available budget.

The DSRD technology transfer to VMI is close to the final stage. A road for the design of the DSRD-based pulser is opened. However the present DSRD technology was not optimized for the specific ILC DR needs. It may need specific modifications in the future.

It was shown in the FNAL mini workshop that the array of the modern programs and projects (based on the accelerator technology) may reap the benefit of the usage of the method where nanosecond high power DSRDs are employed.

Acknowledgements

We would like to thank

- DoE as a sponsor for the SBIR grant
- KEK/SLAC collaboration
- SLAC Klystron Dept
- Ed Cook (for the LLNL board)
- Jon Barth (for the loan of the HV attenuator)