SLAC ILC Damping Ring Kicker High Availability Modulator R&D Program

March 4, 2009

Craig Burkhart

A. Krasnykh, R. Larsen, T. Tang

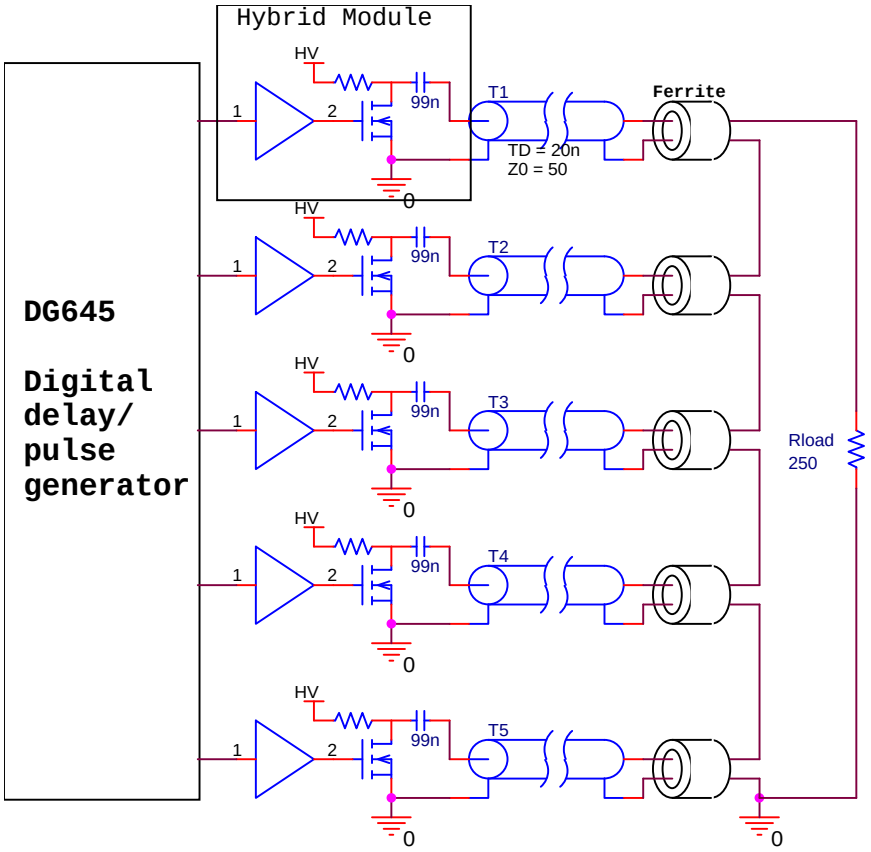
SLAC FY09 R&D Program

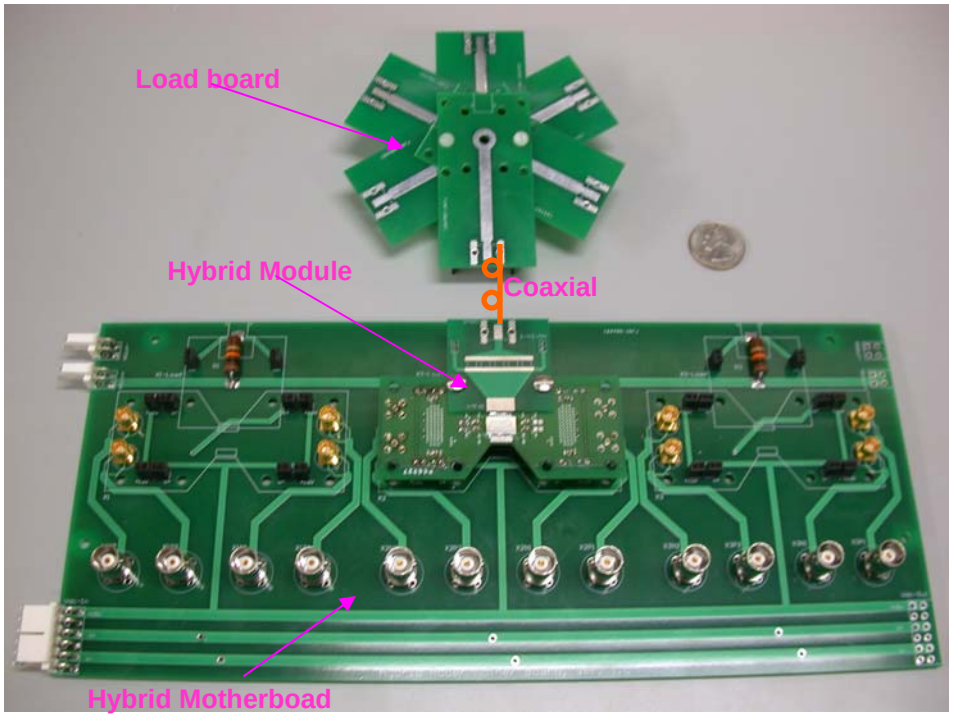
- SLAC program is investigating two approaches
  - MOSFET array (adder) topologies
  - DSRD (opening switch) topologies
- Adder Program
  - “Scale assemblies” to investigate high bandwidth adder topologies with MOSFET/Driver hybrid switches (transmission line adder)
  - ¼ FTE
  - DOE-ILC funding
- DSRD Program
  - DR Kicker modulator for ATF2
  - ¼ FTE
  - US-Japan funding

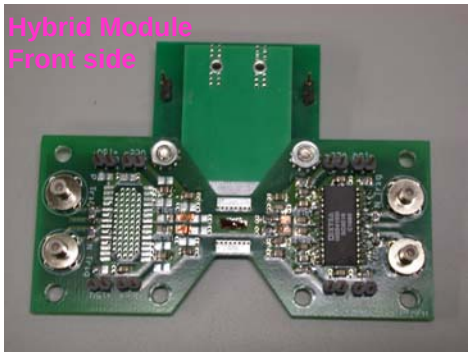
Adder Scale Assemblies

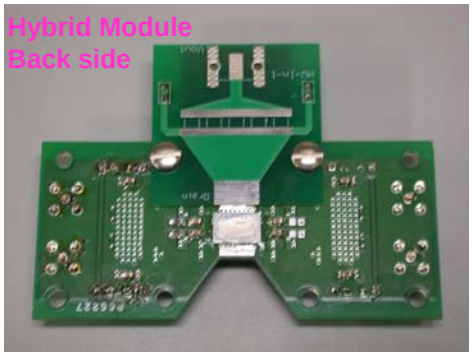
- Transmission line adder
  - Simple, high bandwidth structure
  - Verify preservation of pulse fidelity
  - Inspect for reflections/residual energy
- Adder design
  - Output
    - 5 kV (uni-polar)
    - 250 Ω
  - 5 stages
  - Inductive isolation (alternative inductive adder configuration)
  - Modules incorporate MOSFET/driver hybrid

Adder Assembly







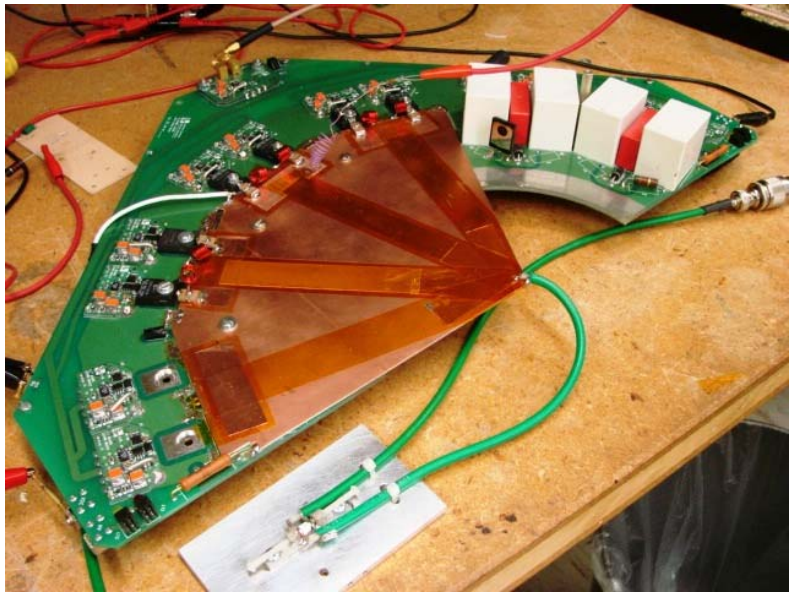


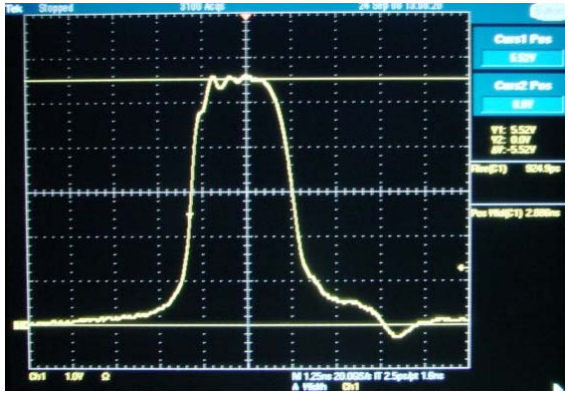
ATF2 DR Kicker Modulator

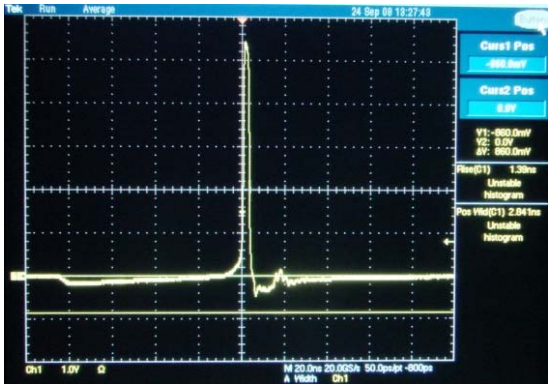
- Parameters
  - Kicker: 60 cm, TEM, bi-polar
  - Output Voltage: ±5 kV
  - Impedance: 50 Ω
  - Pulse Length
    - Flattop: 4 ns
    - Rise/Fall Time: ~1 ns
  - PRF
    - Burst: 3 MHz (1/308 ns nominal, 1/313.6 ns every 3rd pulse)
    - Pulses per Burst: 30
    - Burst PRF: 1.5 Hz
  - Residual Voltage: <50 V (1% of max) after 103.6 ns
- Schedule
  - Brass Board: - 4/09
  - Prototyping: - 7/09
  - Modulator: - 12/09
  - Delivery to KEK: 2010

2-ns Prototype Tests

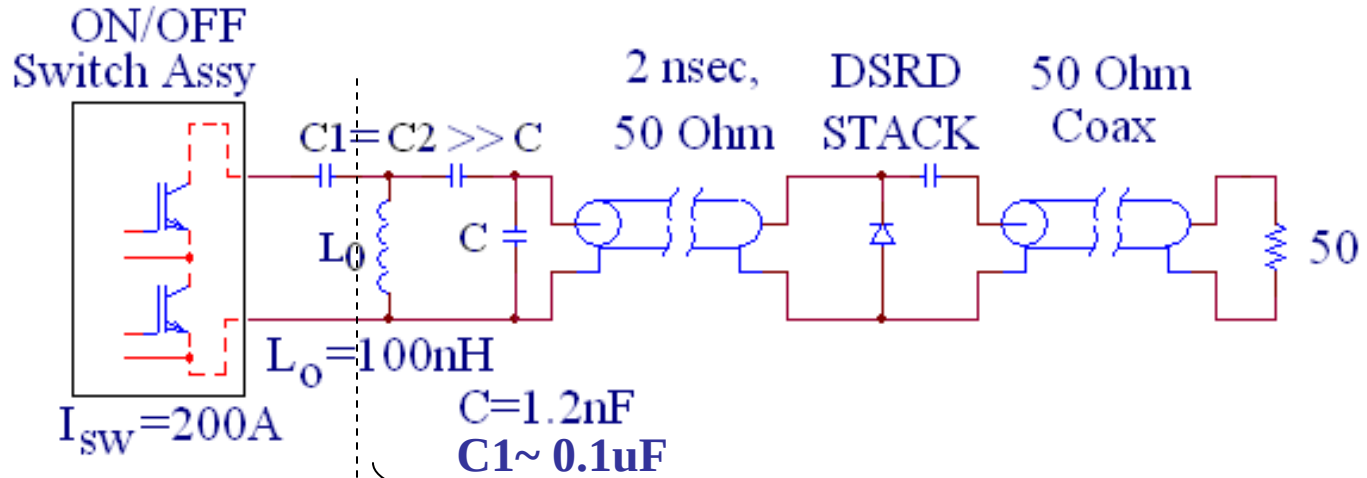
Amplitude	kV	4.4
Impedance of Feeder	Ohm	50
Rise Time	nsec	<1
Pulse Width	nsec	2.9







Focus of current activities



Increase TL to 4 ns, re-tune to minimize pre/post pulse

MOSFETs Drivers

Storage Capacitors

Charging PS

Array of MOSFETs in series and parallel

Reliability of Switch Assembly

Recent Progress

- Developed series MOSFET switch for HV pump
- Received two DSRD from Alexei, optimized for ATF2
- Derived circuit parameters for 4 nsec
- HV 26dB Barth's attenuators for accurate HV measurement
- Received 8-channel trigger generators for control system

Summary

- Adder Program
  - Ultra-fast switching: hybrid circuit achieves fundamental MOSFET limit w/ excellent control
  - Scale adder system under construction
  - Test results during Q3
- DSRD Program
  - Promising results with 2 ns prototype
  - Purchased optimized DSRDs and other required components
  - Focusing on higher power pump development
  - Prototype development Q3/Q4