SiD Electronic Concepts

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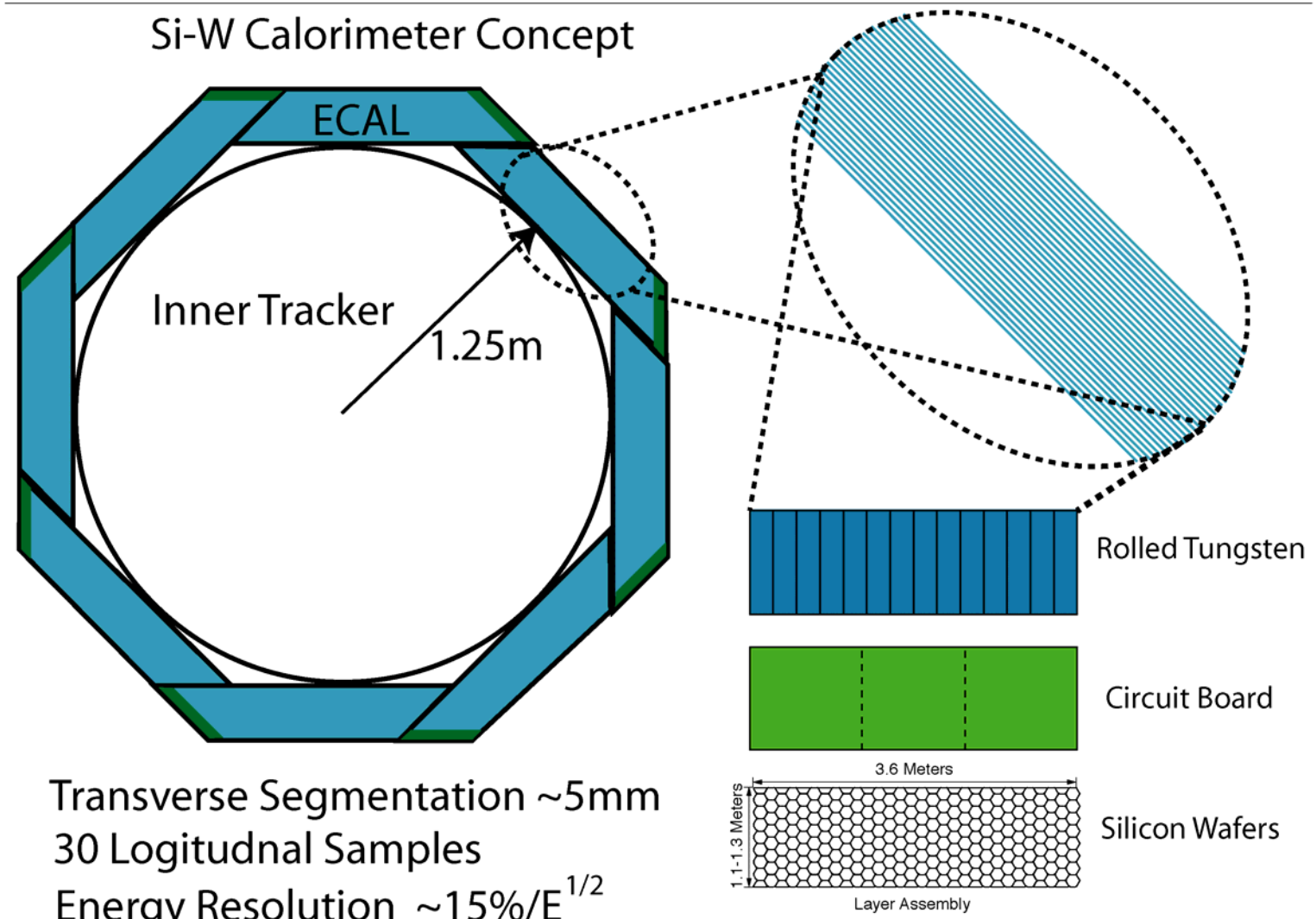
Overview

- SLAC/Oregon/BNL is developing a read out chip (ROC) for the Si-W calorimeter.
  - Highly integrated into structural design – bump bonded to detector
  - 1024 pixels / ROC ---Thus working name KPiX
  - Rough concept for "DAQ" strategy.
- Similar architecture with reduced dynamic range should work for Si strips. 2048 pixels / ROC
- Similar architecture should work for HCal and muon system.
- Will not work for very forward systems.

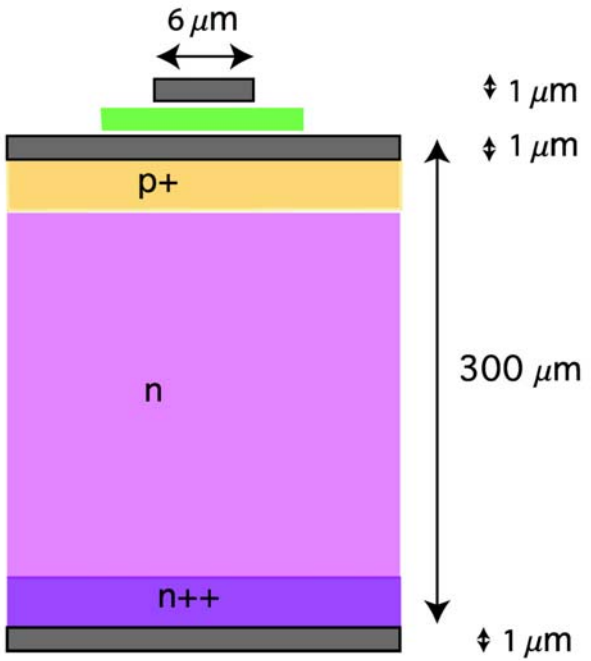
Concept



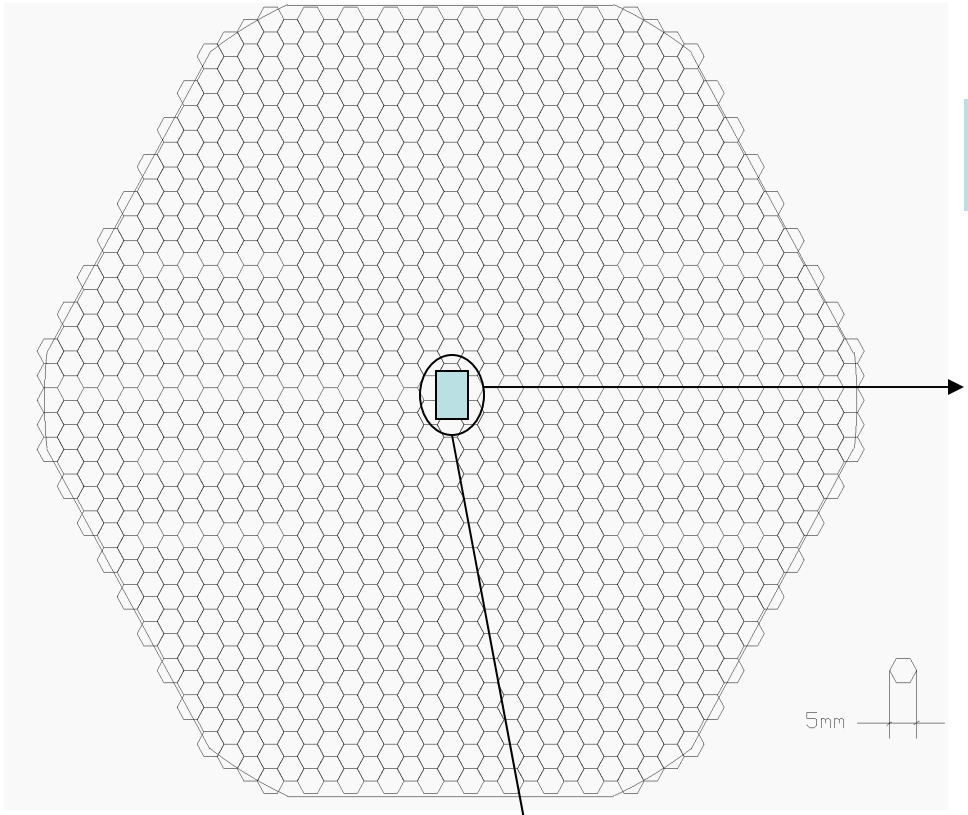
Transverse Segmentation ~5mm
30 Logitudnal Samples
Energy Resolution ~15%/$E^{1/2}$

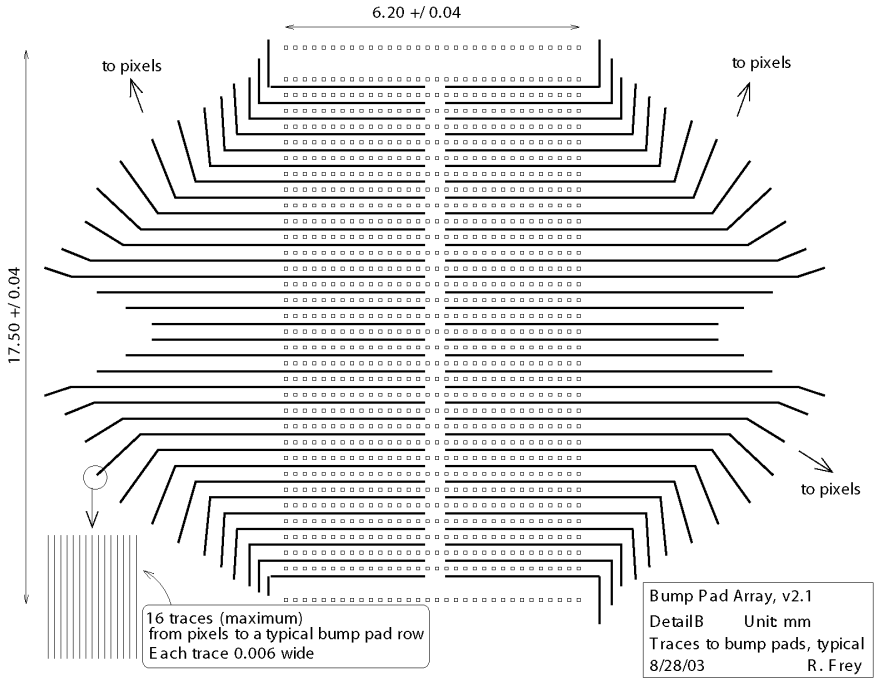
Electronics requirements

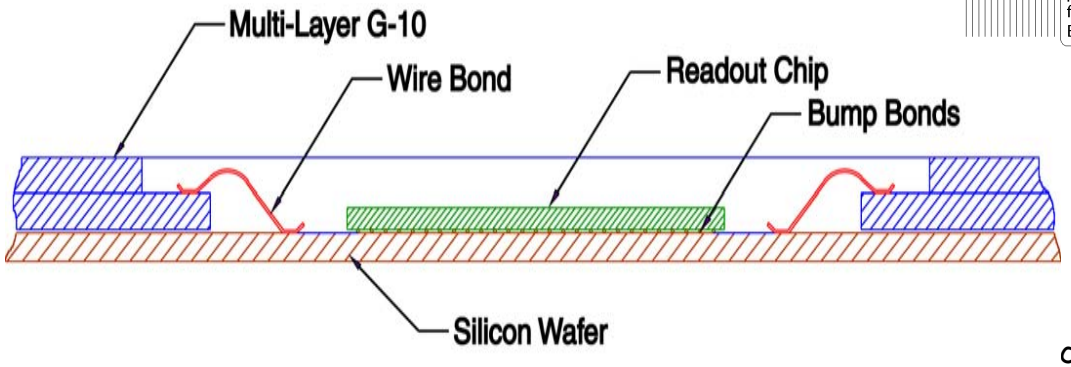
- Signals
  - <2000 e noise
  - Require MIPs with S/N > 7
  - Max. signal 2500 MIPs (5mm pixels)
- Capacitance
  - Pixels: 5.7 pF
  - Traces: ~0.8 pF per pixel crossing
  - Crosstalk: 0.8 pF/Gain x Cin < 1%
- Resistance
  - 300 ohm max
- Power
  - < 40 mW/wafer ⇒ power cycling
    (An important LC feature!)
- Provide fully digitized outputs of charge and time on one ASIC for every wafer.

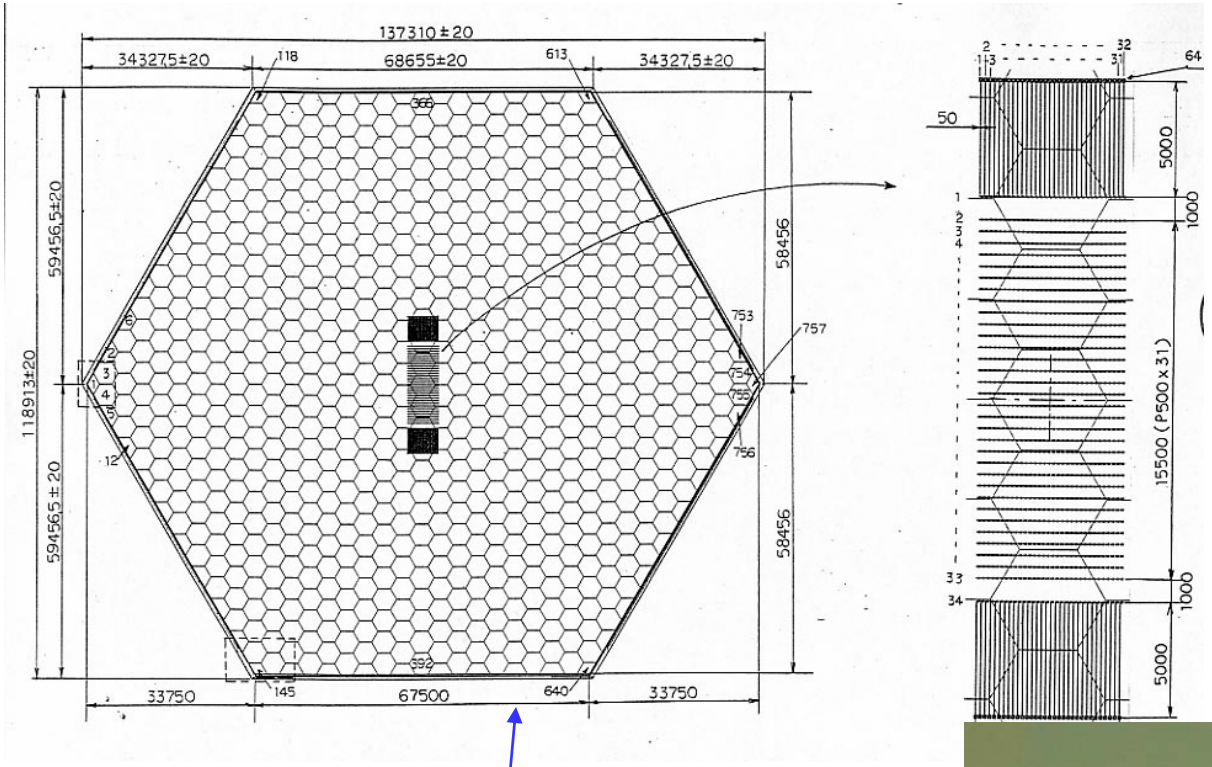


Wafer and readout chip



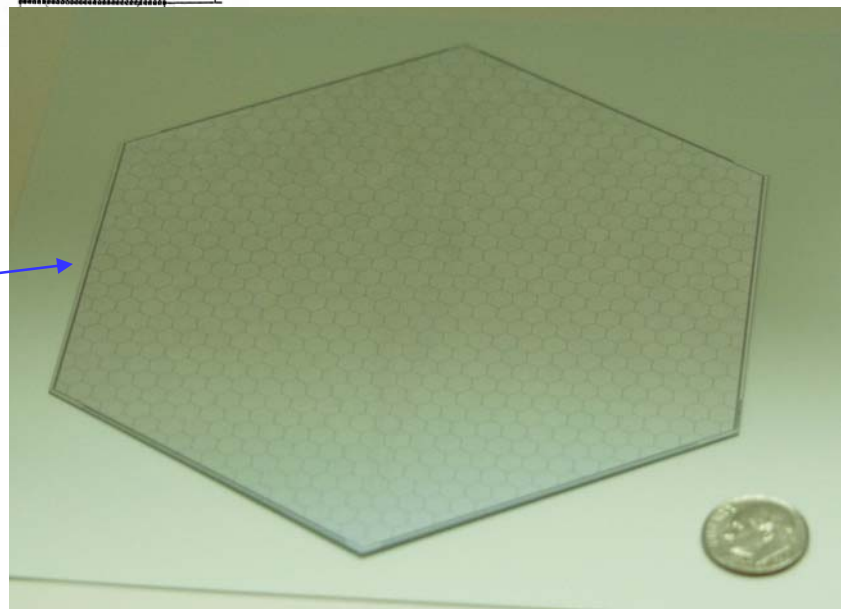


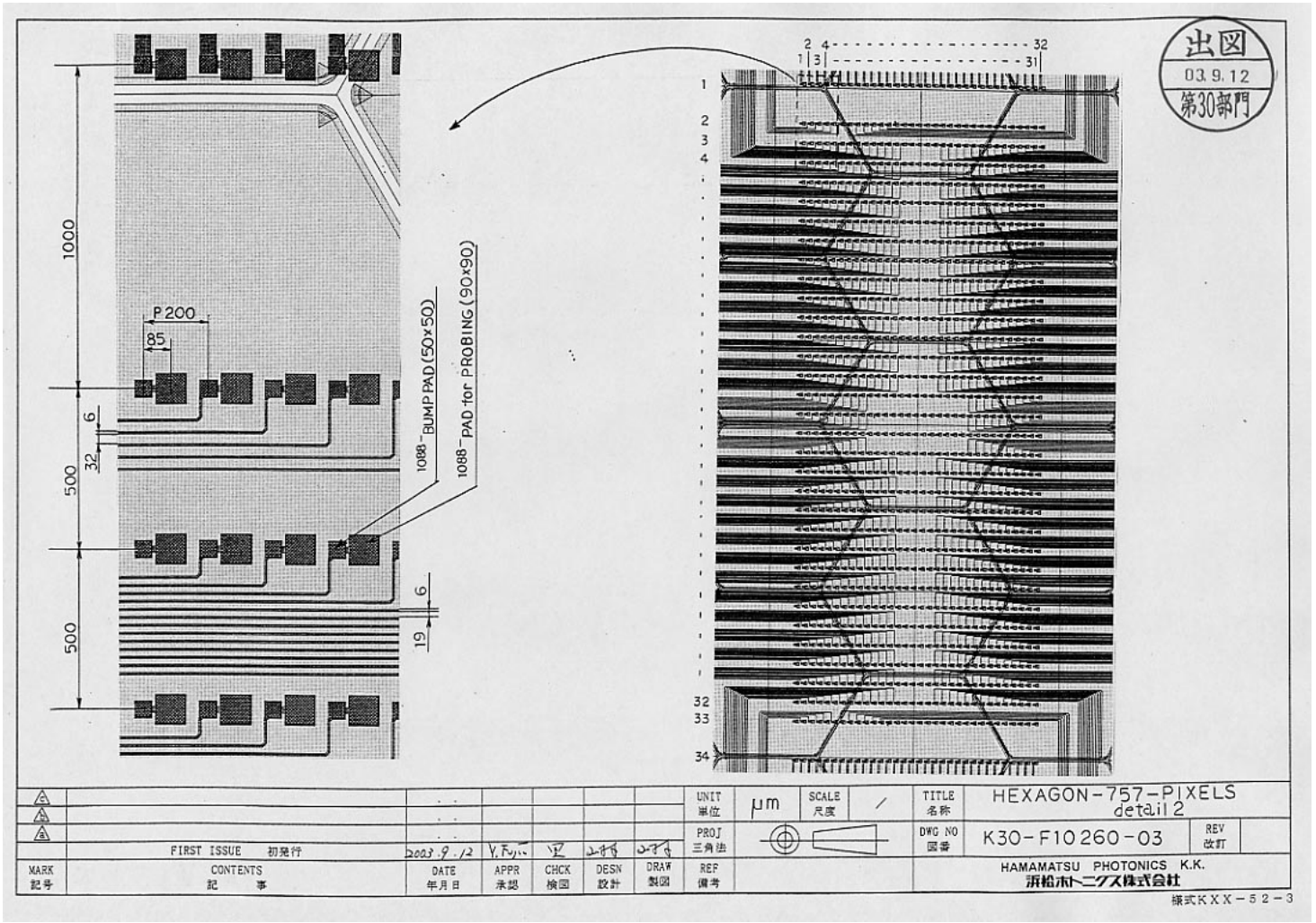




Detector Layout

Real Thing



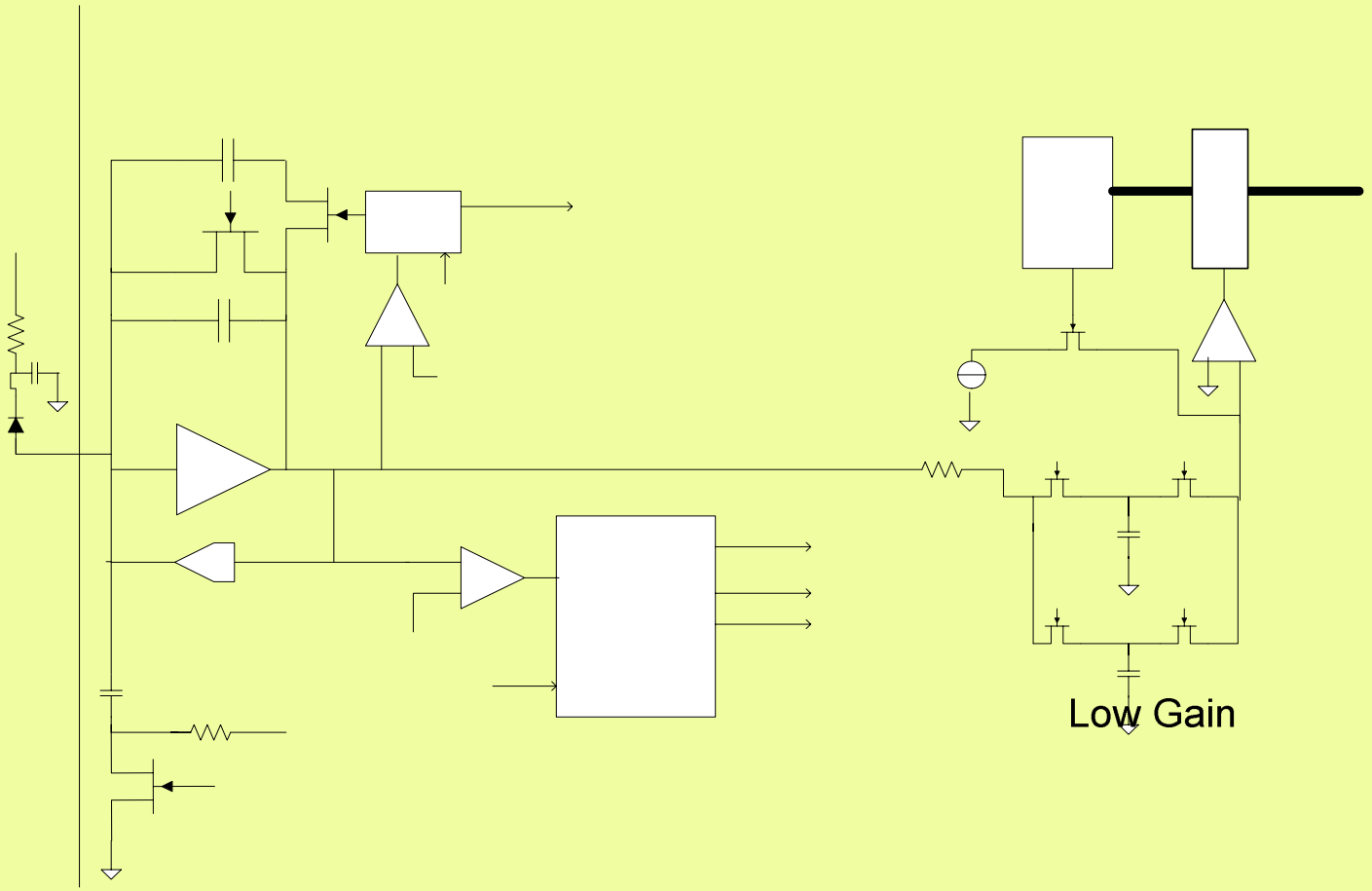

出図
03.9.12
第30部門
P200
85
1000
500
500
6
32
6
19
1088-BUMP PAD (50×50)
1088-PAD for PROBING (90×90)
2
4
32
1
3
31
1
2
3
4
32
33
34
UNIT 単位
μm
SCALE 尺度
TITLE 名称
HEXAGON-757-PIXELS detail 2
PROJ 三角法
DWG NO 図番
K30-F10260-03
REV 改訂
FIRST ISSUE 初発行
2003.9.12
Y.Fujii
MARK 記号
CONTENTS 記事
DATE 年月日
APPR 承認
CHCK 検図
DESN 設計
DRAW 製図
REF 備考
HAMAMATSU PHOTONICS K.K.
浜松ホトニクス株式会社
様式KXX-52-3

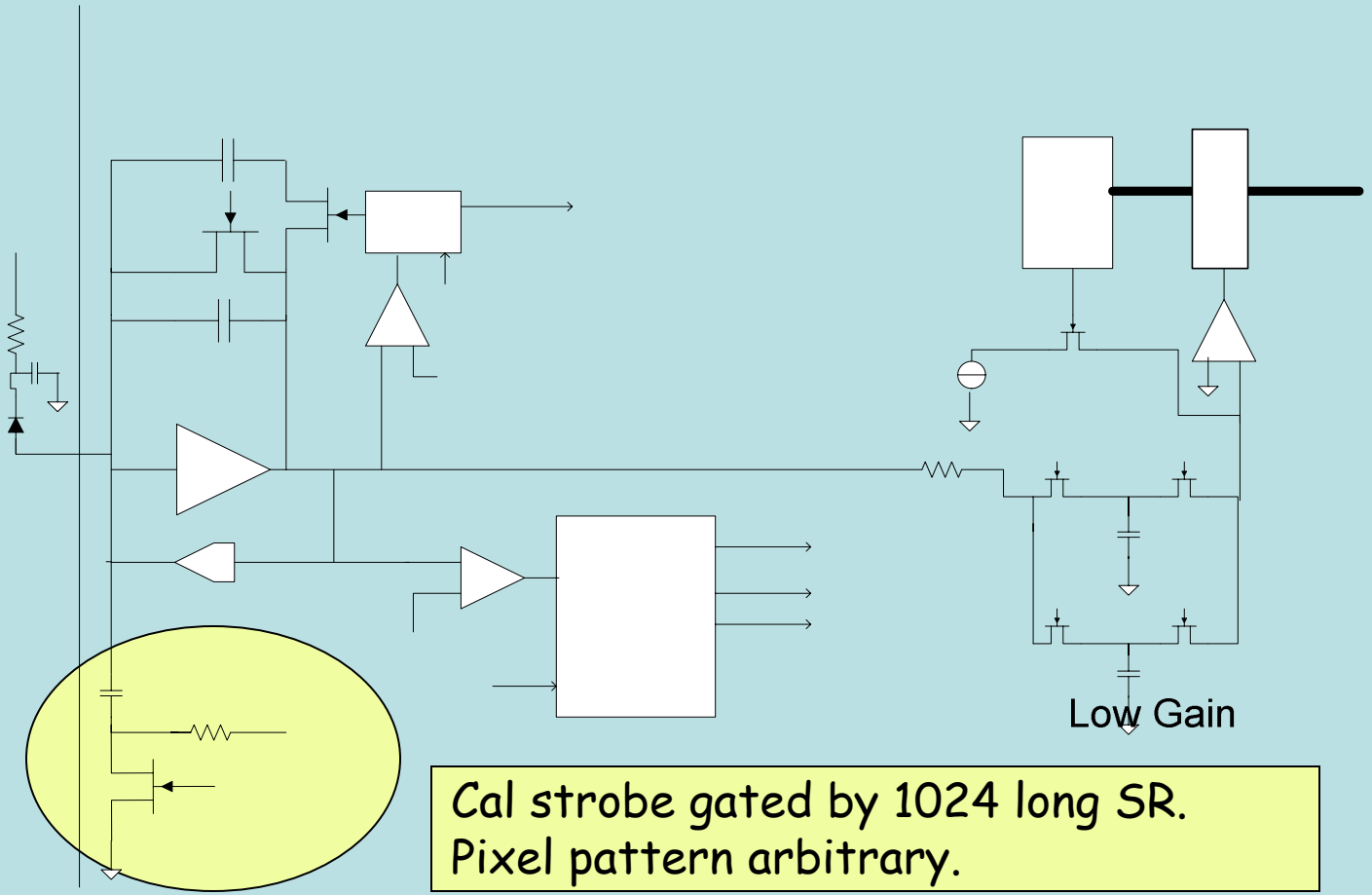
Conceptual Design of W-SI Front-End ASIC

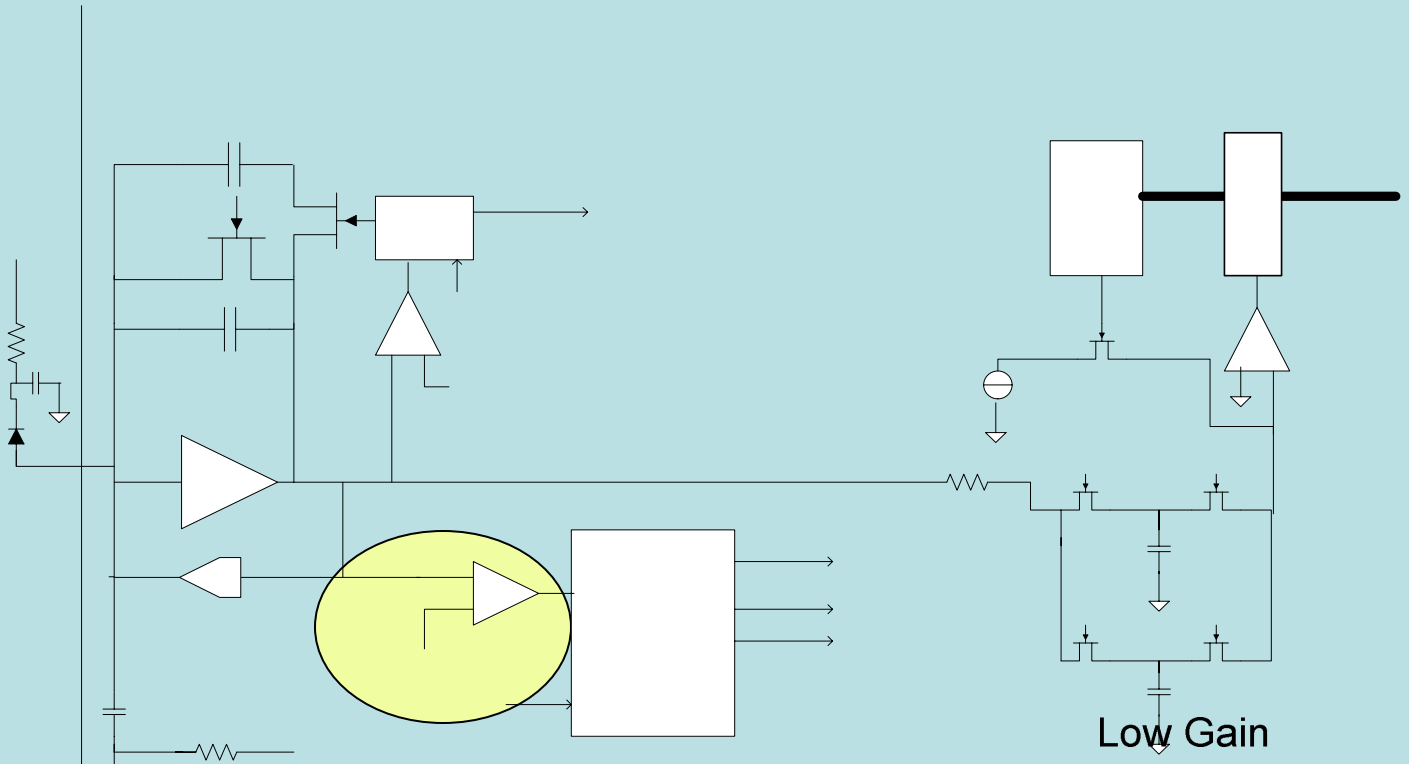
	Document #	Date Effective
		12/15/2004
	Prepared by(s)	Supersedes
	Breidenbach/Freytag/Haller/Milgrome	None
Project Name	Subsystem/Office	
Document Title		
Conceptual Design of W-SI Front-End ASIC		

Version 1.3

There is an 18 page technical document, now in its 4th major revision for register assignments, etc for the cold bunch structure.


Low Gain
Reset


Low Gain
Cal strobe gated by 1024 long SR.
Pixel pattern arbitrary.
Reset



Event discriminator implemented as limiter followed by discriminator. Limiter holds off resets, permitting longer integration time for discriminator and data hold. Discriminator threshold selected from either of two ROC wide DAC's.

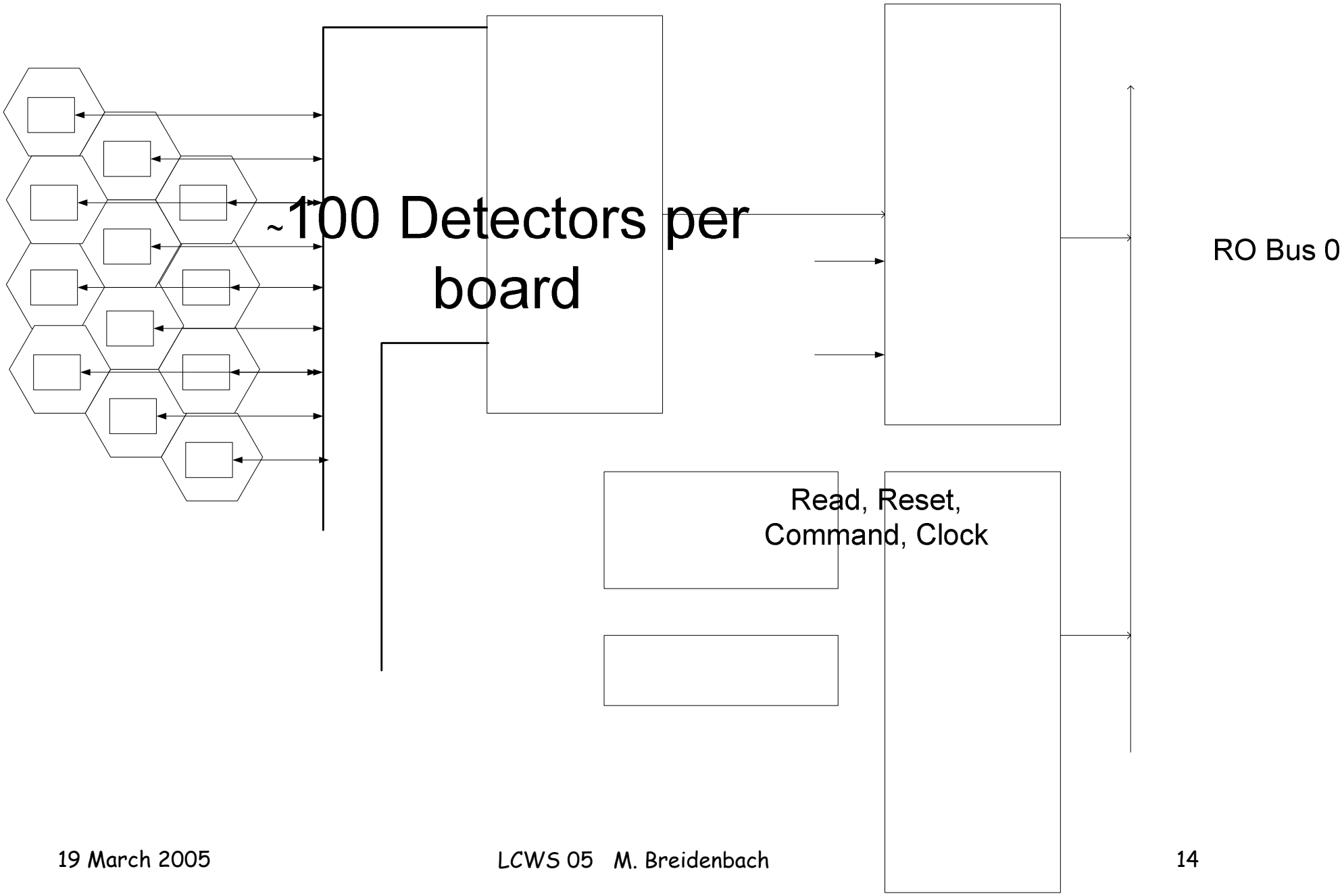
Pulse "Shaping"

- Take full advantage of synchronous bunch structure:
  - Reset (clamp) feedback cap before bunch arrival. This is equivalent to double correlated sampling, except that the "before" measurement is forced to zero. This takes out low frequency noise and any integrated excursions of the amplifier.
  - Integration time constant will be 0.5 – 1 μsec. Sample *synchronously* at 2 – 3 integration time constants.
  - Time from reset 1 – 3 μsec, which is equivalent to a 1 – 3 μsec differentiation.

- Noise: ~1000 e^- for ~ 20 pF. (100 μA through input FET).

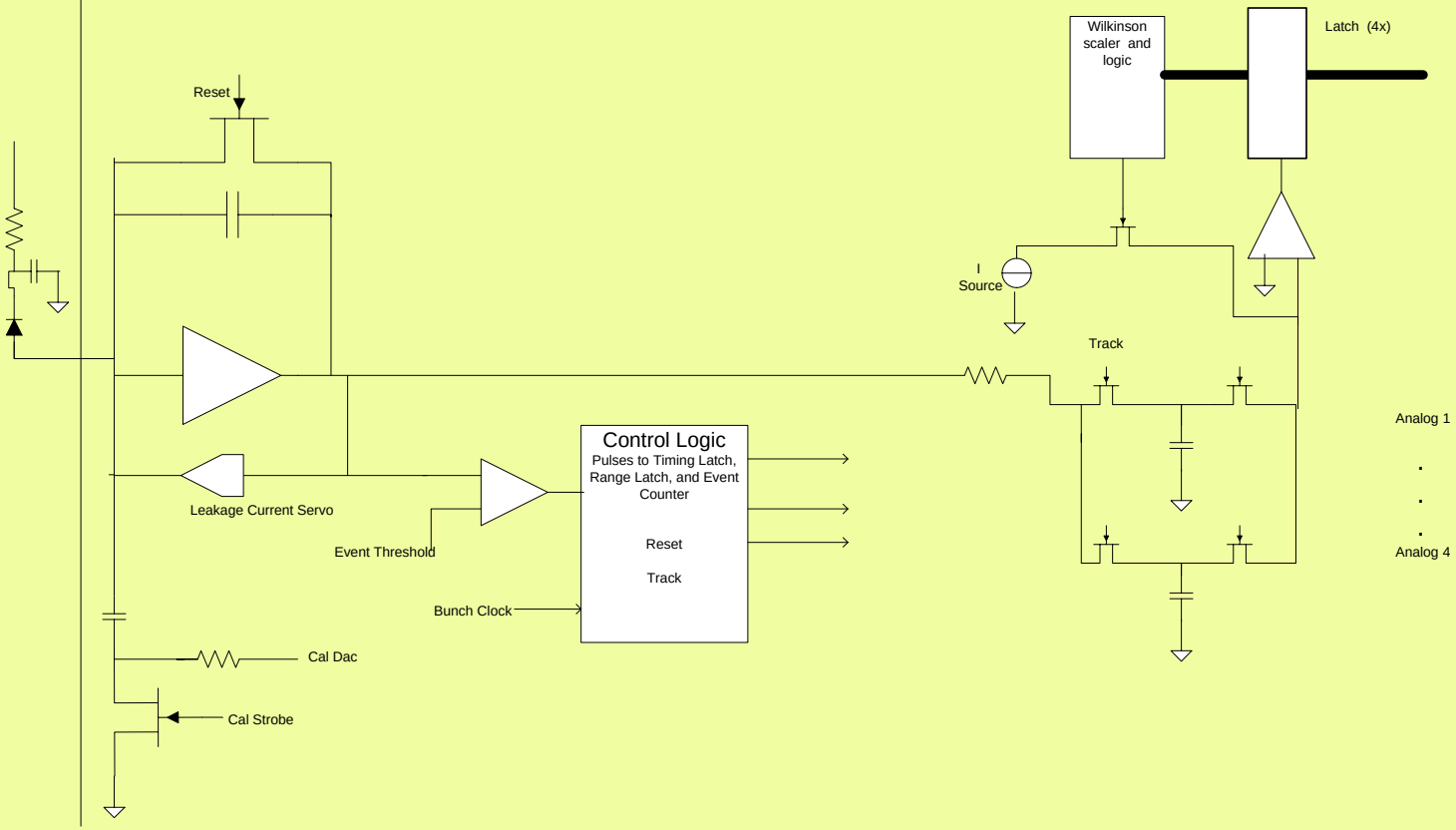
Power

			Cold Train/Bunch Structure				
Phase	**Current (ma)**	**Instantaneous Power (mw)**	**Time begin (us)**	**Time End (us)**	**Duty Factor**	**Average Power (mw)**	**Comments**
All Analog "on"	370.00	930.00	0.00	1,020.00	5.10E-03	4.7	Power ok with current through FET's
Hold "on", charge amp off	85.00	210.00	1,021.00	1,220.00	9.95E-04	0.2	
Analog power down	4.00	10.00	1,020.00	200,000.00	9.95E-01	9.9	
LVDS Receiver, etc		3.00	0.00	200,000.00	1.00E+00	3.0	Receiver always on.
Decode/Program		10.00	1.00	100.00	4.95E-04	0.0	Sequencing is vague!
ADC		100.00	1,021.00	1,220.00	9.95E-04	0.1	
Readout		50.00	1,220.00	3,220.00	1.00E-02	0.5	
Total						18.5	Total power OK


~100 Detectors per board
RO Bus 0
Read, Reset,
Command, Clock

Tracker Pixel Analog Section

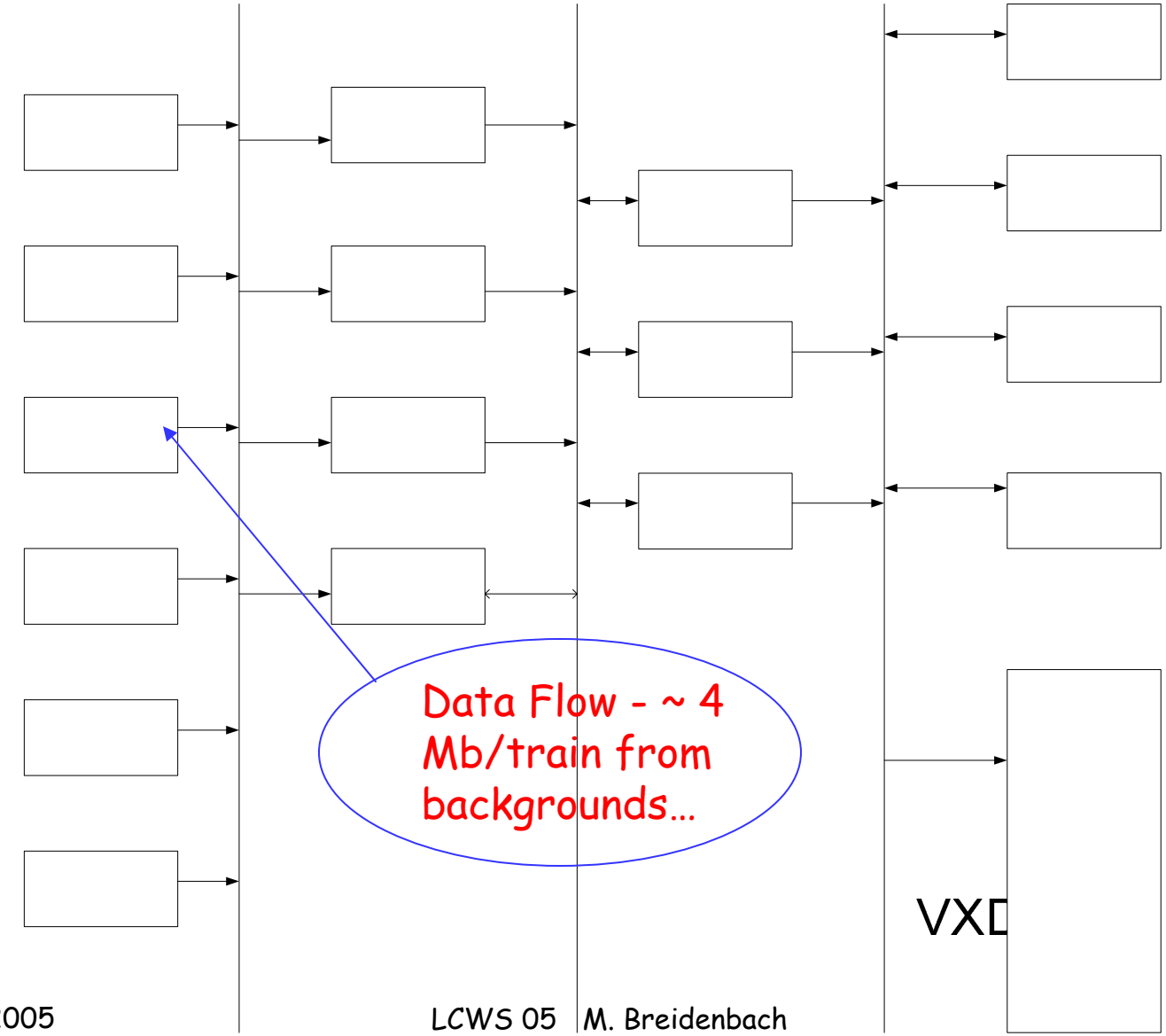
1 of 2048 pixels



Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit) and Event Counter (5 bits).
Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.


Data Flow - ~ 4 Mb/train from backgrounds…
VXD

Comments

- The basic architecture should work with all the low occupancy sub-systems.
  - Including Tracker, EmCal, HCal, and muon system.
  - It does not address VXD issues – presumably CMOS to be developed – or the completely occupied Very Forward Calorimeters.
  - A variant might work in the forward regions of the tracker and calorimeters.
- The architecture is insensitive to the bunch separation within a train.
- The cost of a mask set is high, so development will be with (probably) 8 x 8 subsets instead of the 32 x 32 array.
- The unit cost of a large number of chips seems fine - <~ $40.
- Substantial design and simulation is done on EMCal Readout chip. Layout is progressing.
- ~No work done on anything else.