First Results with the Prototype Detectors of the Si/W ECAL

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- Physics Design Requirements
- Detector Concept
- Silicon Detectors Capacitance and Trace Resistance
- Implications of Accelerator Technology Choice
- MIPS, sources and laser

Si-W work – personnel and responsibilities

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Electronics, Mechanical Design, Simulation	Si Detectors , Mechanical Design, Simulation	Electronics

* This work includes contributions from Oregon students Tyler Neely and Eric Fitzgerald.

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ECAL Design Requirements

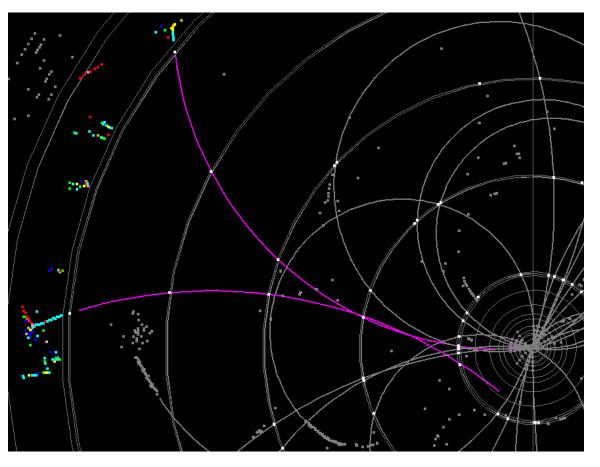
- Optimal contribution to the reconstruction of multijet events:
 - Excellent separation of γ 's from charged particles Efficiency > 95% for energy flow
 - Excellent linkage of ECAL with tracker (important for SiD)
 - Good linkage of ECAL with HCAL
 - Good reconstruction of π^{\pm} , detection of neutral hadrons
 - Reasonable EM energy resolution (< 15%/ \sqrt{E})

Physics case: jet reconstruction important for many physics processes.

• Longitudinal Sampling, 30 layers needed for EM energy resolution $\frac{\sigma_E}{E} \sim 20\% \sqrt{\frac{X}{E}}$ X is the sampling in radiation length.

• Useful for K^0 tracking, etc.

• Can tolerate small, random inefficiency



See talks by Eckhard von Toerne

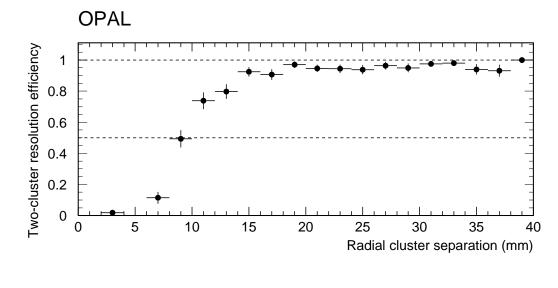
Importance of Granularity

• Figure of merit for energy reconstruction is

$$f_E \simeq rac{max(R_M, 4d)}{R_{cal}}$$

where R_M is the Molière radius, d is the detector pad size and R_{cal} is the inner radius of the calorimeter (factor of 4 somewhat arbitrary)

Example (OPAL SiW luminosity monitor, $1X_0$ radiator, 3mm gap)



d= 2.5mm , $R_M\sim$ 17mm

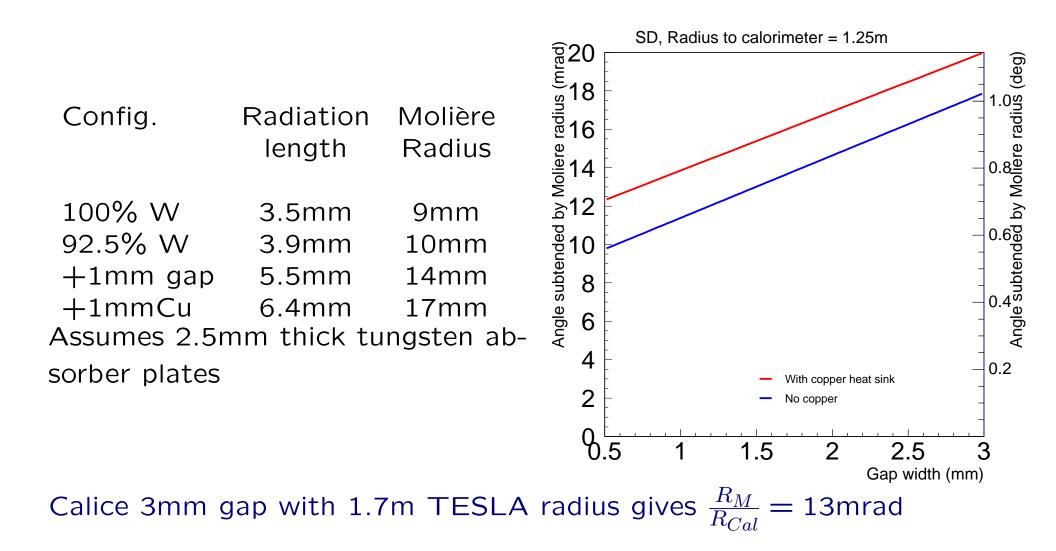
• The costs of the calorimeters, coil, and muon system have

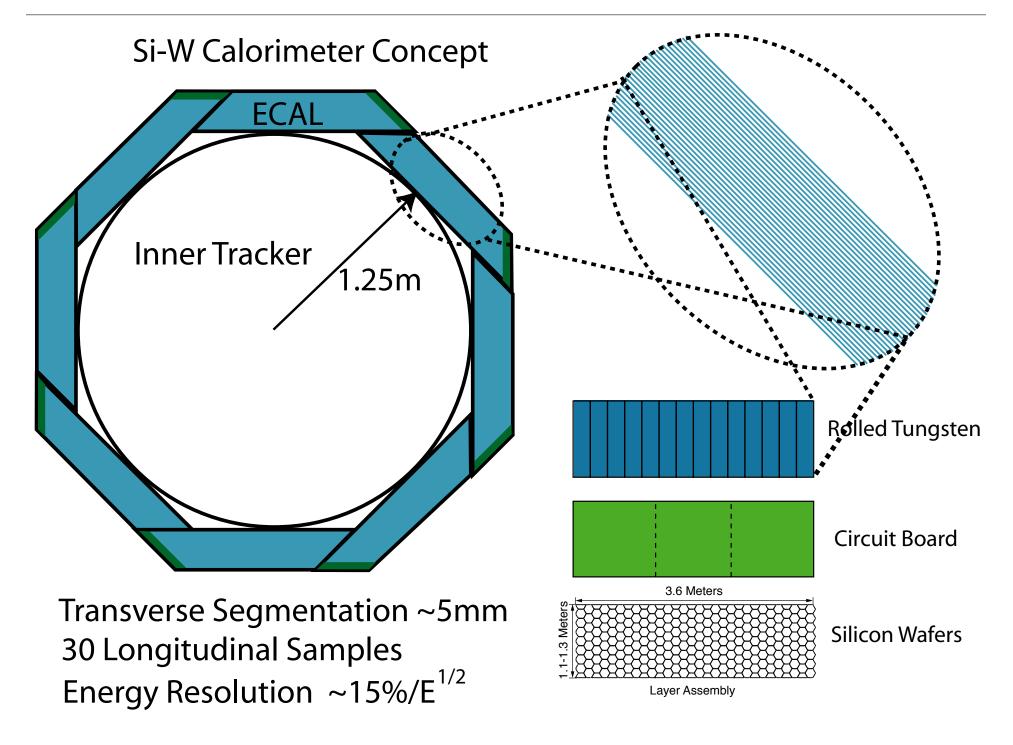
 $cost \propto R_{cal}^n$

where *n* is $\sim 2 - 3$.

- Thus a 10% increase in the Molière radius of the calorimeter leads to a > 20% increase in cost of the detector for constant f_e .
- Conclusion: try and make the calorimeter as dense as possible

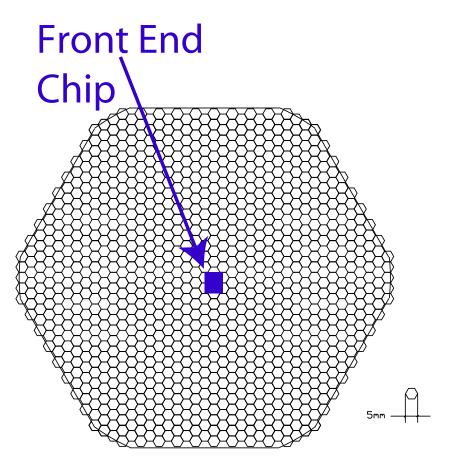
Critical parameter: gap between tungsten layers.





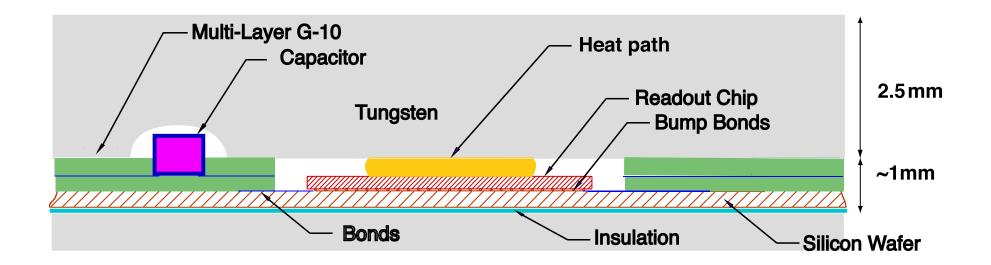
Silicon Concept

- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of front end chip
- May want different pad layout in forward region



6 inch (152mm) Dia Wafer

Critical parameter: minimum space between tungsten layers.



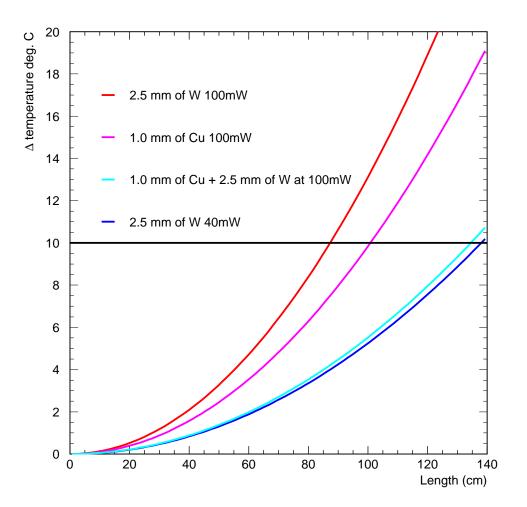
Evolving capacitor packaging may eliminate need for dimples.

Can we get the heat out?

Back of the envelope calculation of change in temperature:

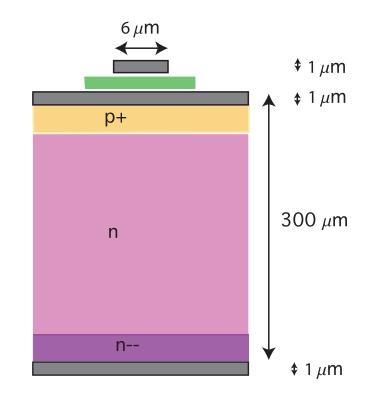
- Thermal Conductivity of W alloy 120W/(K-m)
- Thermal Conductivity of Cu 400W/(K-m)

Need to reduce heat to below 100mW/wafer.

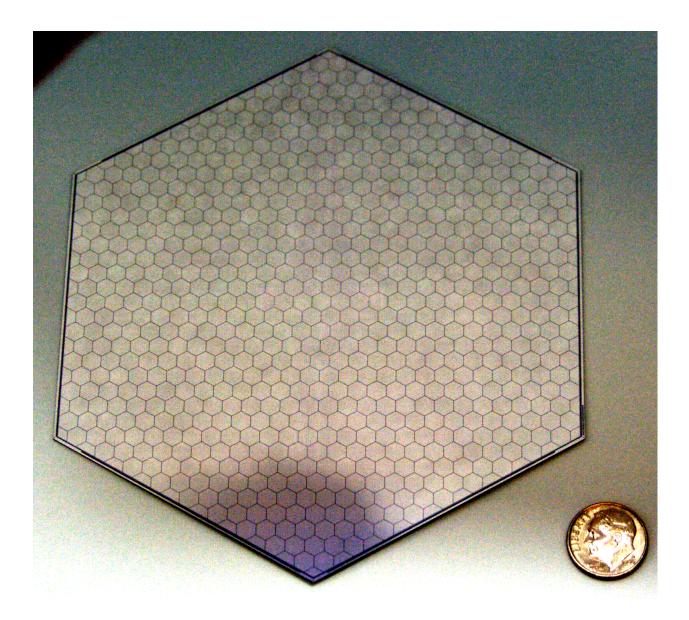


Silicon Detector Design

- DC coupled detectors (avoids bias resistor network)
- Two metal layers
- Keep Si design as simple as possible to reduce cost
- Cross talk looks small with current electronics design
- Trace capacitances (up to 30pF) are bigger than the 5pF pixel capacitance



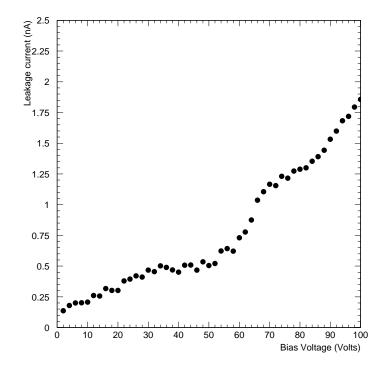
Ten Hamamatsu detectors are in hand



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Measurements on Silicon Detector Prototypes

Leakage Current Looks Fine:



(10nA for 1μ s gives only 250 electrons noise) NB: Neighboring pixels are not grounded. Expected contributions to detector capacitance:

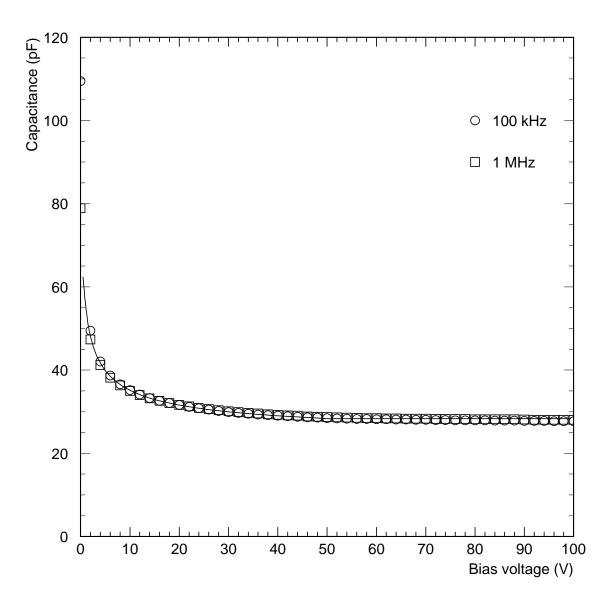
- 5.7pF from pixel capacitance (C_{geom})
- ~ 20pF for sum of trace capacitance and capacitance from other traces connecting to other pixels. (C_{stray})
- Pixels under the bump-bond array have additional stray capacitance from probing and bonding pads (currently $\simeq 100 \text{pF}$)

Expected curves

$$C_{tot} = C_{stray} + C_{geom} \sqrt{\frac{V_{dep} + V_{bi}}{V_{bias} + V_{bi}}} \qquad V_{bias} < V_{dep}$$

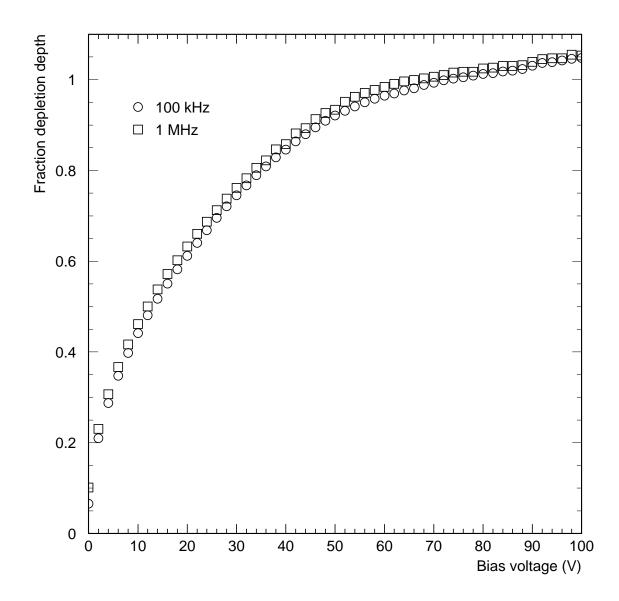
$$C_{tot} = C_{stray} + C_{geom} \qquad V_{bias} > V_{dep}$$

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Typical CV curve as measured in lab

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Relative depletion depth as a function of voltage.

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Mean stray capacitance measurement obtained from a fit to the CV curve:

Expected 100kHz 1 MHz

 23.0 ± 0.2 pF $~21\pm1$ pF $~22\pm1$ pF

 \Rightarrow Measurement agrees with expectation for 0.9 μ m thick oxide and 6 μ m wide traces (3.1 pF/cm).

Series resistance for 1 μ m by 6 μ m :

Expected (pure AI) Measured

 $47 \ \Omega/cm \qquad (57\pm2)\Omega/cm$

 \Rightarrow Measurement slightly larger than nominal

Impact of Detector Technology on Detector Design

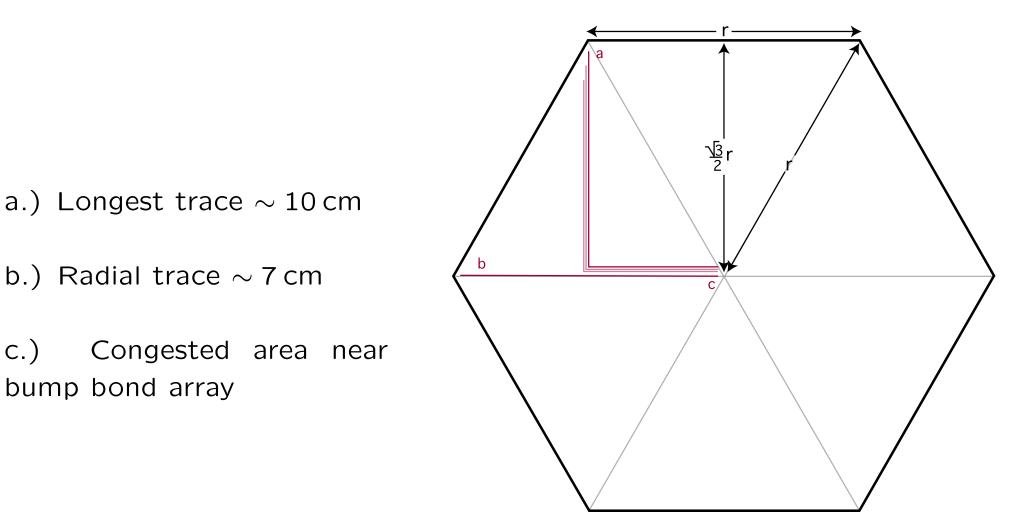
 \Rightarrow In a warm machine, exceptional pixels with large capacitance or series resistance lead to degraded time tag measurements

• Small impact on tagging performance since bad channels can be deweighted in determining the average time of a track

 \Rightarrow In a cold machine, exceptional pixels with large capacitance or series resistance lead to a higher rate of noise events in buffers

• Could lead to inefficiency late in the bunch train due to buffer overflow

Location of high resistance and capacitance pixels



C.)

• For areas *a* and *b* fundamental limit to noise is given by (for e.g. correlated double sampling)

$$ENC_{R_s} \sim C_{tot} \sqrt{4 \frac{KT}{q_e^2} R_s \frac{1}{2\tau}}$$

where R_s is the series resistance, C_d and τ is the shaping time of the electronics.

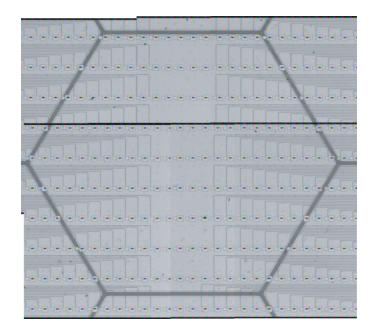
• For $\tau = 1\mu s$, $R_s = 580 \Omega$ and $C_{tot} = 40 \, pF$ this gives ~ 600 electrons noise, which is not really a problem.

• We can slightly improve noise performance by decreasing the trace width, perhaps by a factor of 2, i.e.

$$ENC_{R_s} \propto \sqrt{w}$$

where w is the trace width.

• In region c, near the bump bonding array, we will have a large number of traces crossing a pixel. No series resistance, but amplifier FET noise similar:



Possible ways to decrease capacitance in region c:

- Move probing pads on to pixels.
- Decrease trace width in area near central pixels, here

 $ENC_{amp} \propto w$

• Use a long skinny chip (e.g. 100 μ m x 600 μ m grid) After these three measures, worst case capacitance is ~70 pF. Other more radical alternatives

- Polyimide (kapton) can be used instead of SiO₂ as insulator for traces
- Oxide thickness to 5μ m possible.
- Minumum trace with probably $10\mu m$
- Could reduce stray capacitances by a factor of 2 or more

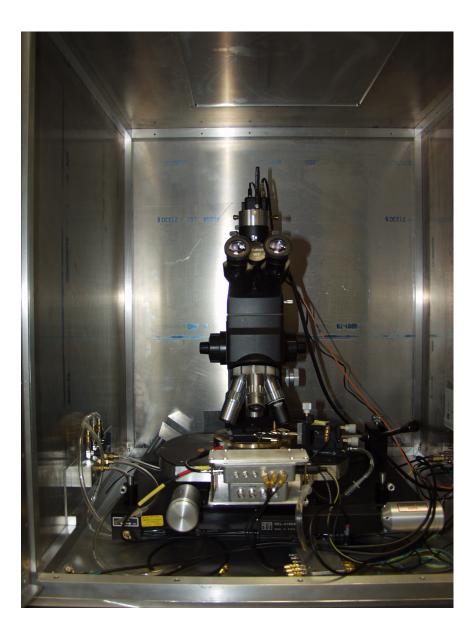
Hamamatsu does not currently provide metal-on-polyimide products, but we could increase the thickness of the wafer and the SiO_2 .

SINTEF (Norway) may be producing detectors based on 6 inch wafers with metal-on-polyimide within the next year. (Possible collaboration with Brookhaven to produce masks.)

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Test Setup for Cosmics, Sources and Laser

- Modified probe station, allows laser to be target on entire detector
- \bullet IR microscope objective used to focus laser to $\sim 10\,\mu{\rm m}$ spot
- Bias applied to backside of detector using insulated chuck



Test Setup – detector probing

 Contact made to test pads on bump bonding array using an AC probe

• Cables add \sim 20 pF of additional capacitance, but noise performance is somewhat better than readout chip

• Use AMPTEK 250F preamp, shapers with $\tau \simeq 1 \mu s$ and a digitizing oscilloscope to mockup expected electronics

• PC board with $1 \text{ cm} \times 1 \text{ cm}$ silicon pad detector used for cosmic trigger visible under chuck Response of detectors to Cosmics (Single 5mm pixel) Simulate LC electronics (noise somewhat better)

width = 780 electrons

10⁴

10³

 10^{2}

10

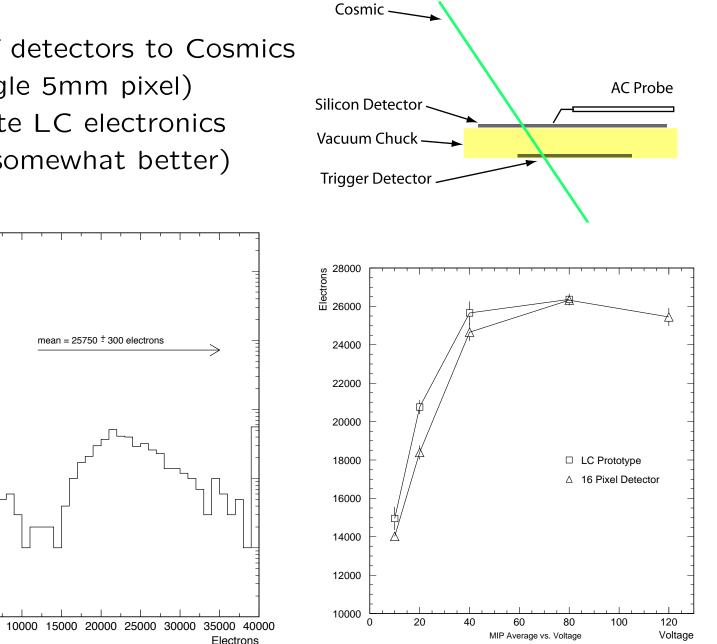
1

10

-5000

0

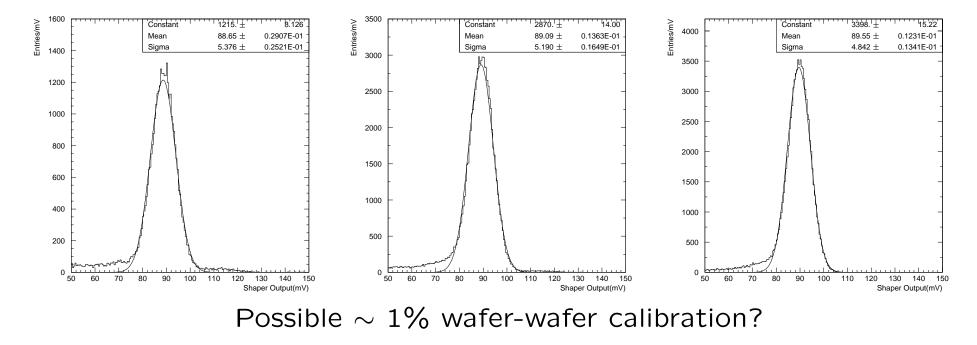
5000



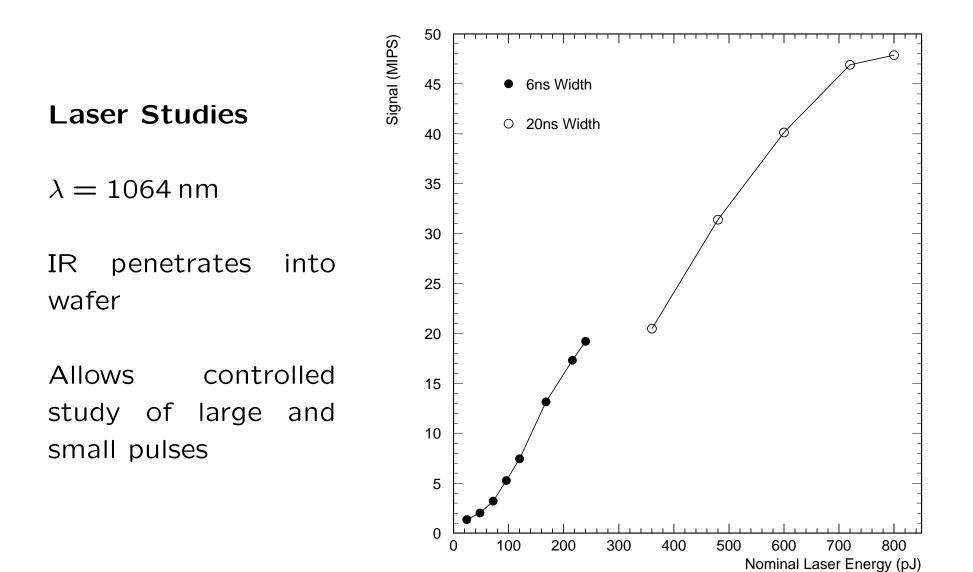
Errors do not include $\sim 10\%$ calibration uncertainty (no source calibration)

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Response of Detectors to 60KeV Gamma's from Am²⁴¹



Width of distributions corresponds to \sim 970 electrons noise. Pixels under test are on outer edge of wafer – includes larger series resistance contribution than cosmic data.



Conclusions

- A narrow gap silicon-tungsten detector for LC physics is attractive
- First round of prototype silicon detectors perform as expected
- Detectors can be produced with workable values of stray capacitance and series resistance
 - \Rightarrow some changes need for cold design