Progress towards a Long Shaping-Time Readout for Silicon Strips

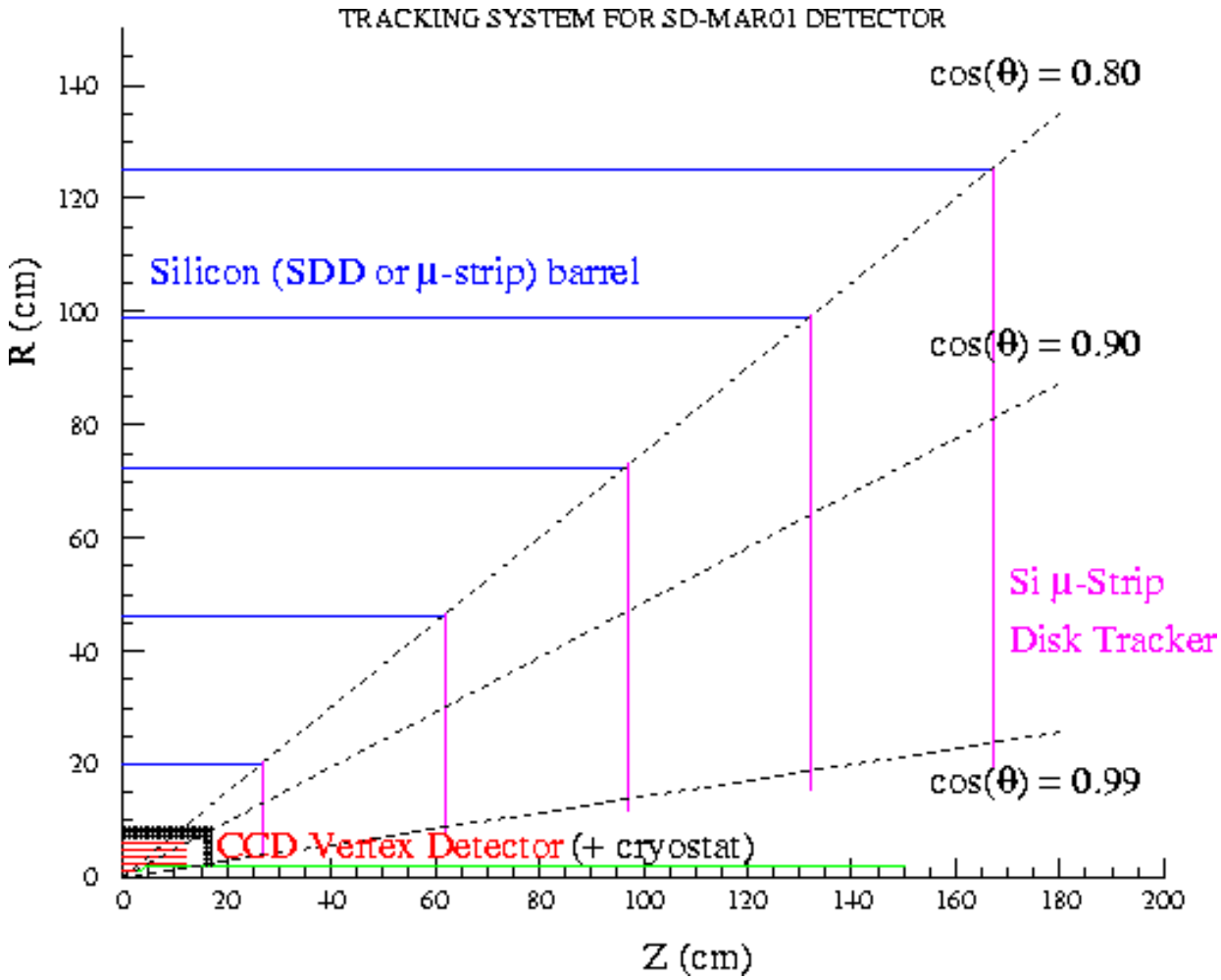
Bruce Schumm

SCIPP & UC Santa Cruz

Victoria Linear Collider Workshop

July 28-31, 2004

The SD Tracker



Idea: Noise vs. Shaping Time

Agilent 0.5 μm CMOS process (qualified by GLAST)

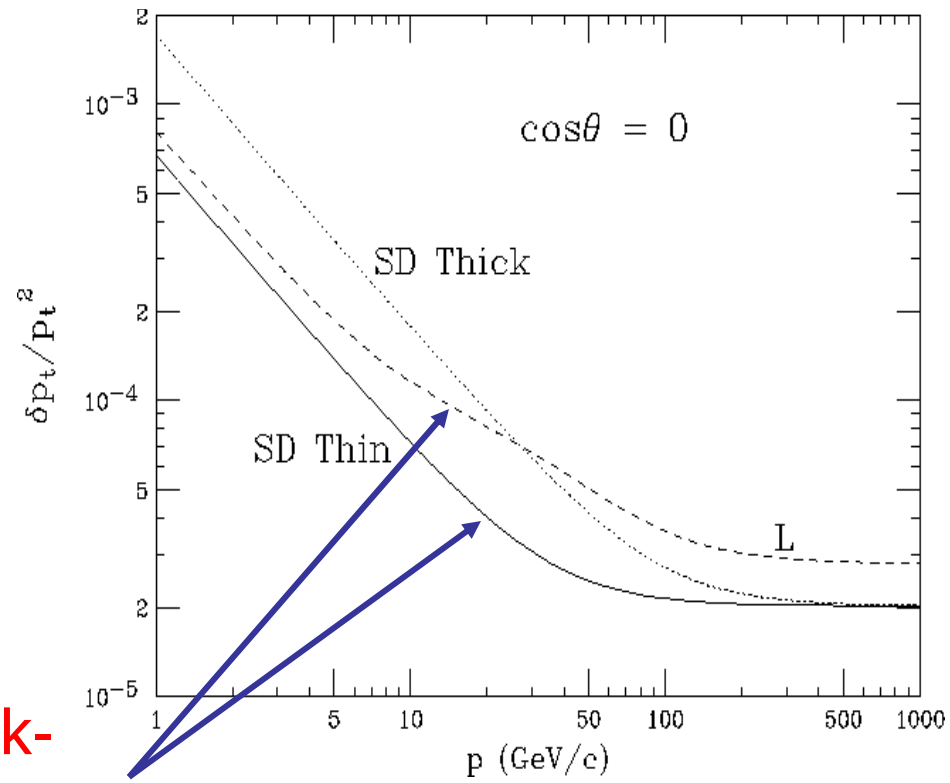
Min-i for 300μm Si is about 24,000 electrons

Shaping (μs)	Length (cm)	Noise (e^-)
1	100	2200
1	200	3950
3	100	1250
3	200	2200
10	100	1000
10	200	1850

The Gossamer Tracker

Ideas:

- Long ladders ➔ substantially limit electronics readout and associated support
- Thin inner detector layers
- Exploit duty cycle ➔ eliminate need for active cooling



➔ Competitive with gaseous tracking over full range of momenta

Also: forward region...

The SCIPP/UCSC Effort

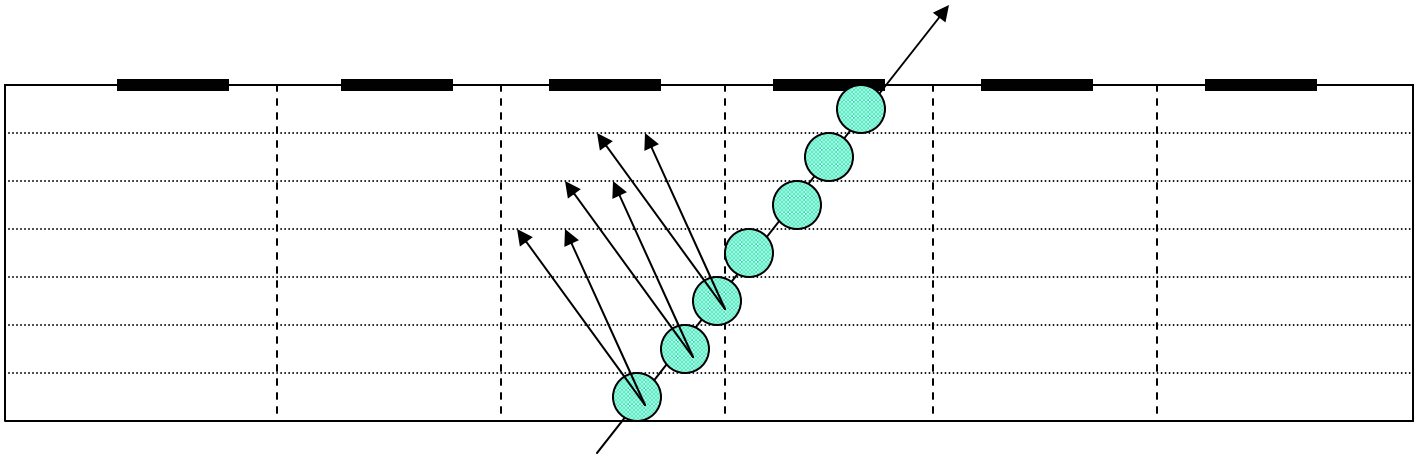
Faculty/Senior	Post-Docs	Students
Alex Grillo	Gavin Nesom	Christian Flacco
Hartmut Sadrozinski	Jurgen Kroseberg	Michael Young
Bruce Schumm		
Abe Seiden		

Engineer: Ned Spencer

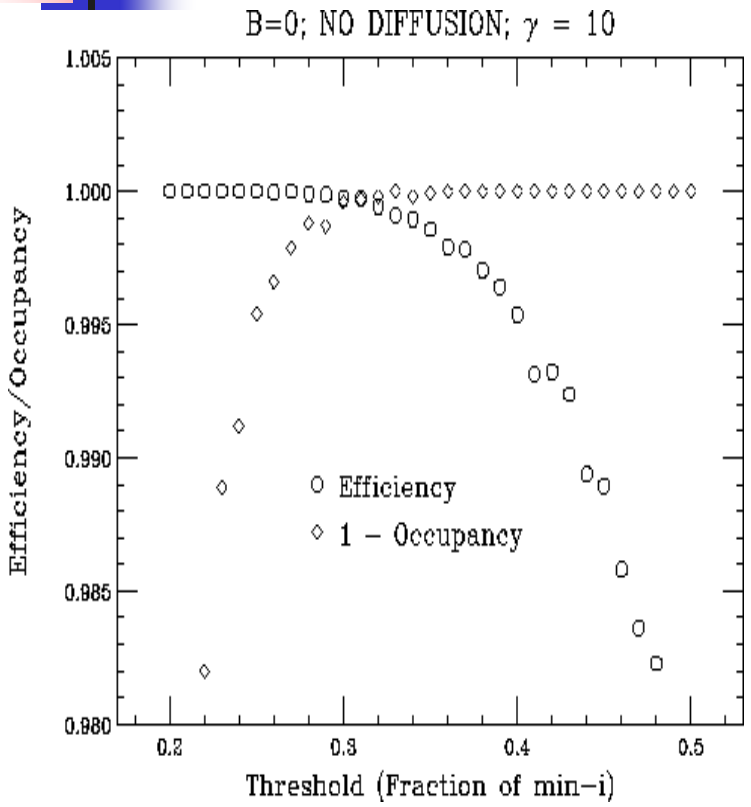
Pulse Development Simulation

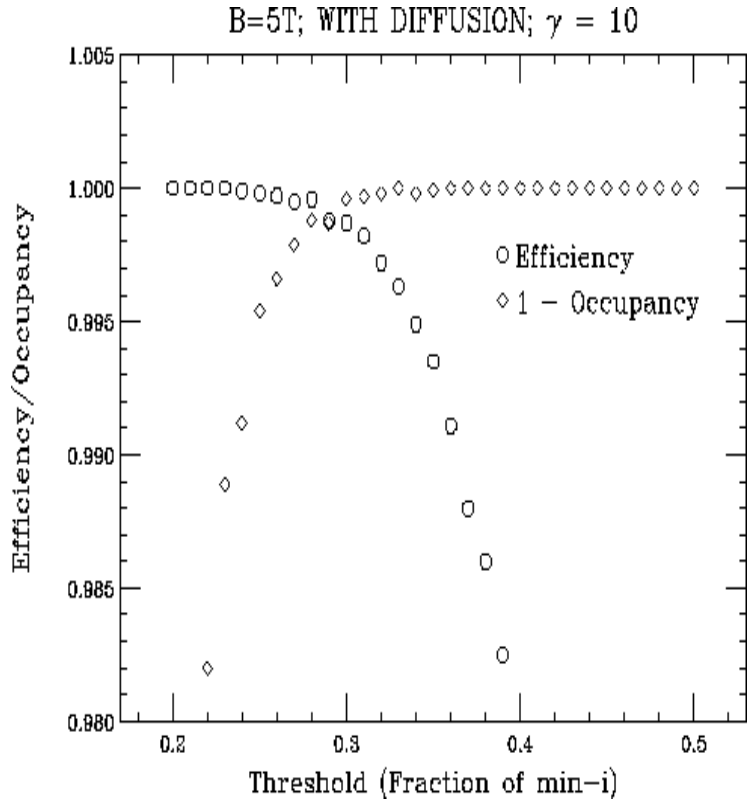
Long Shaping-Time Limit: strip sees signal if and only if hole is collected onto strip (no electrostatic coupling to neighboring strips)

Incorporates: Landau statistics (SSSimSide; Gerry Lynch LBNL), detector geometry and orientation, diffusion and space-charge, Lorentz angle, electronic response



Result: S/N for 167cm Ladder





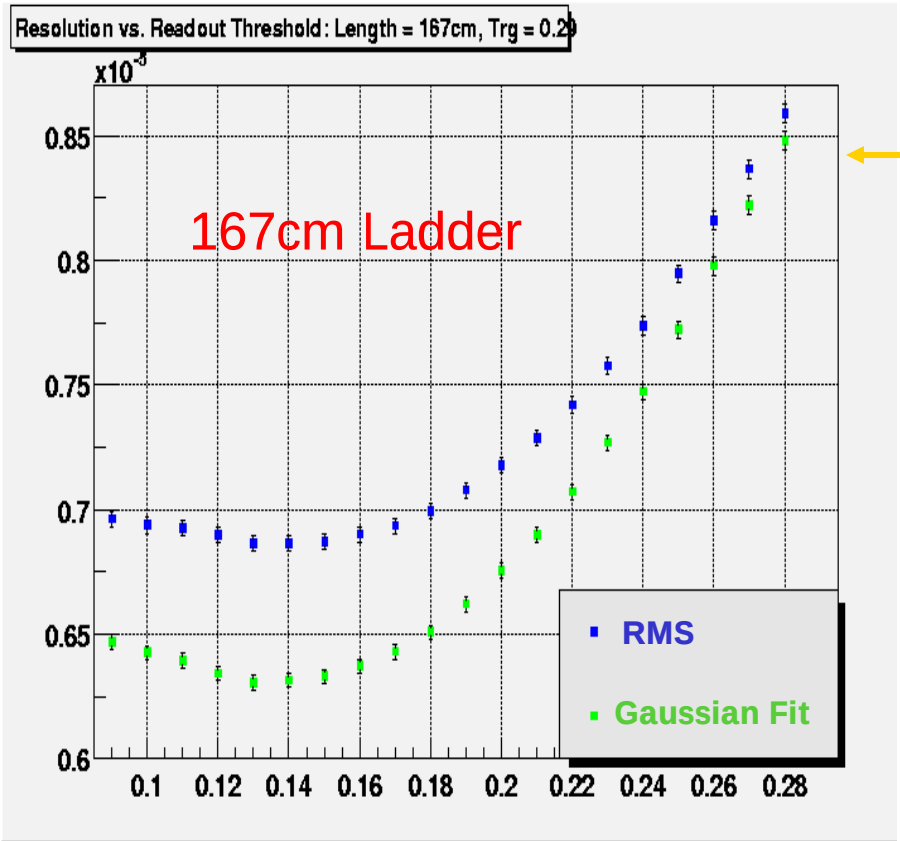
At shaping time of 3μs; 0.5 μm process qualified by GLAST

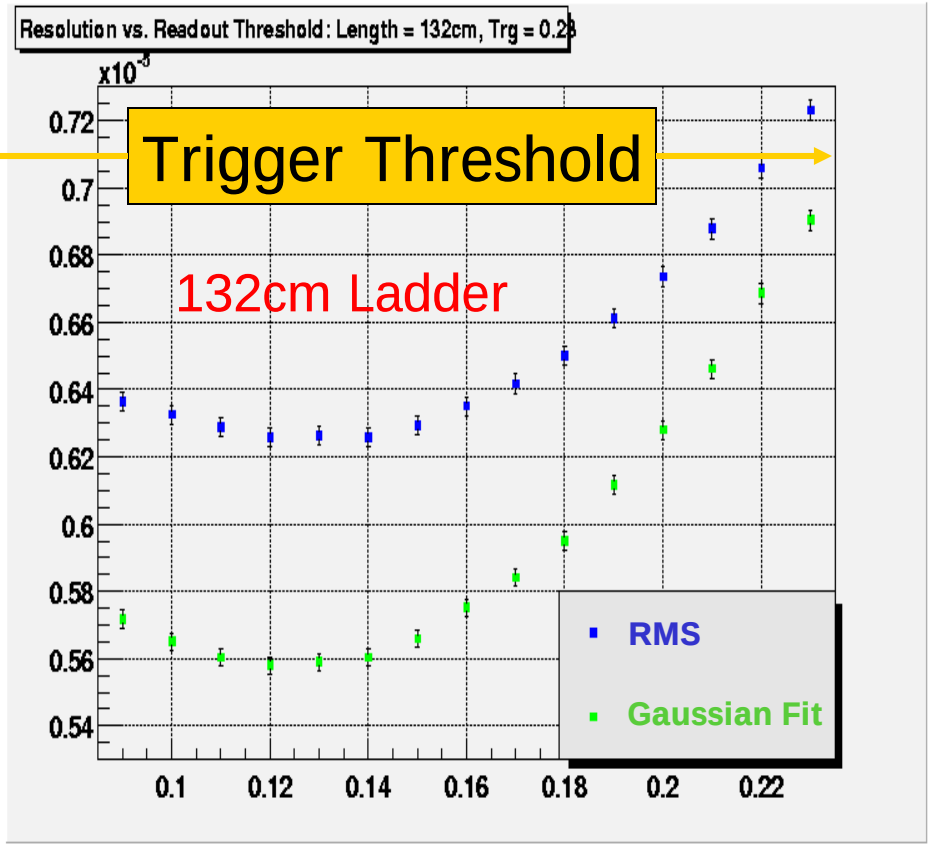
Single-Hit Resolution

Design performance assumes 7μm single-hit resolution. What can we really expect?

- Implement nearest-neighbor clustering algorithm
- Digitize time-over-threshold response (0.1*τ more than adequate to avoid degradation)
- Explore use of second `readout threshold' that is set lower than `triggering threshold'; design implication

Resolution With and Without Second (Readout) Threshold

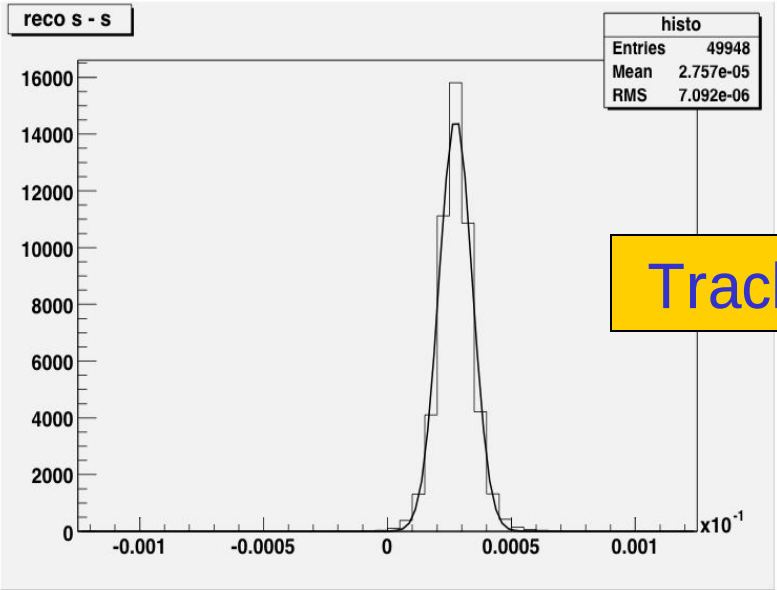




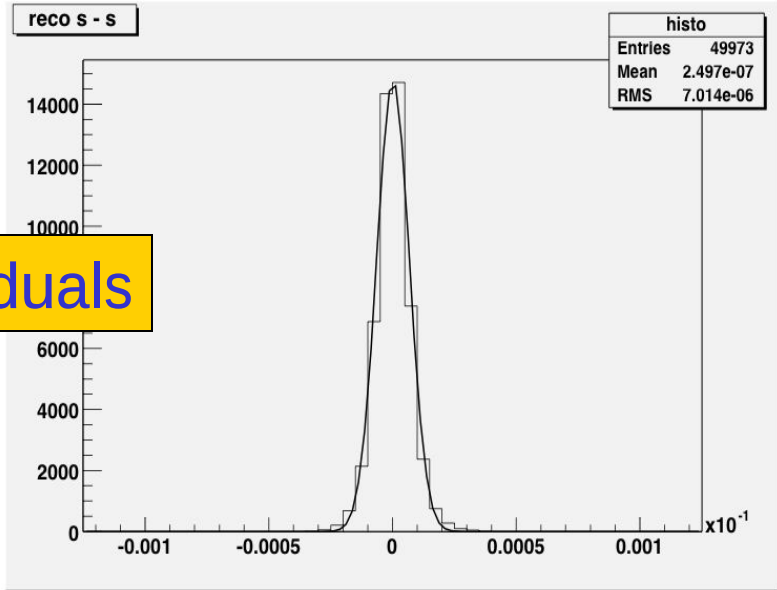
Readout Threshold (Fraction of min-i)

Faking the Magnetic Field

Michael Young, UCSC



Track Residuals

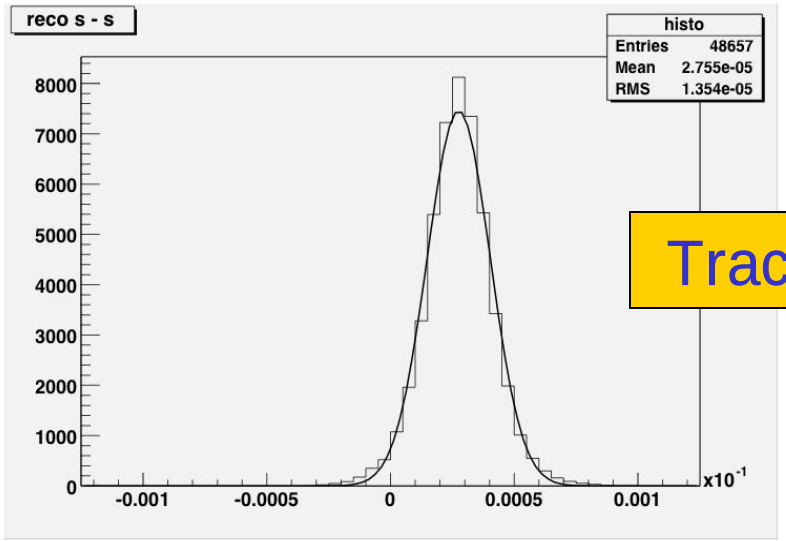


B = 5 T; straight-through track

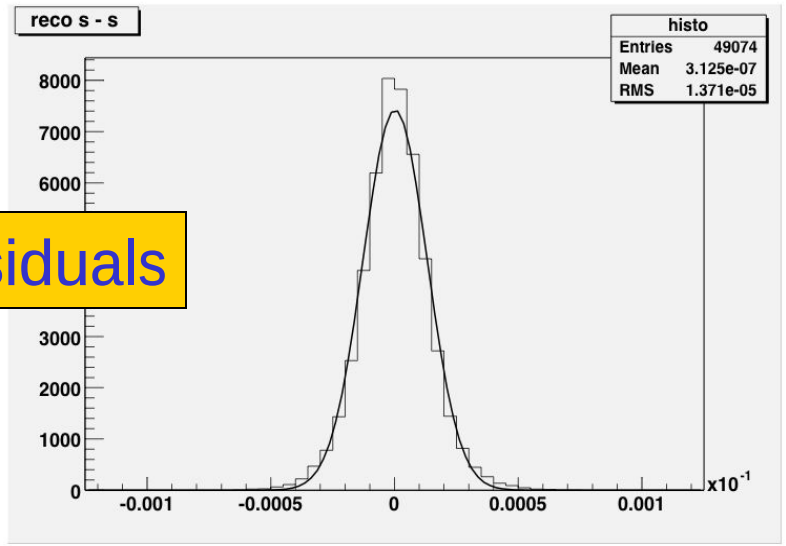
B = 0; 180 mrad tilt (Lorentz angle for 5T)

Faking the Magnetic Field

Michael Young, UCSC



Track Residuals

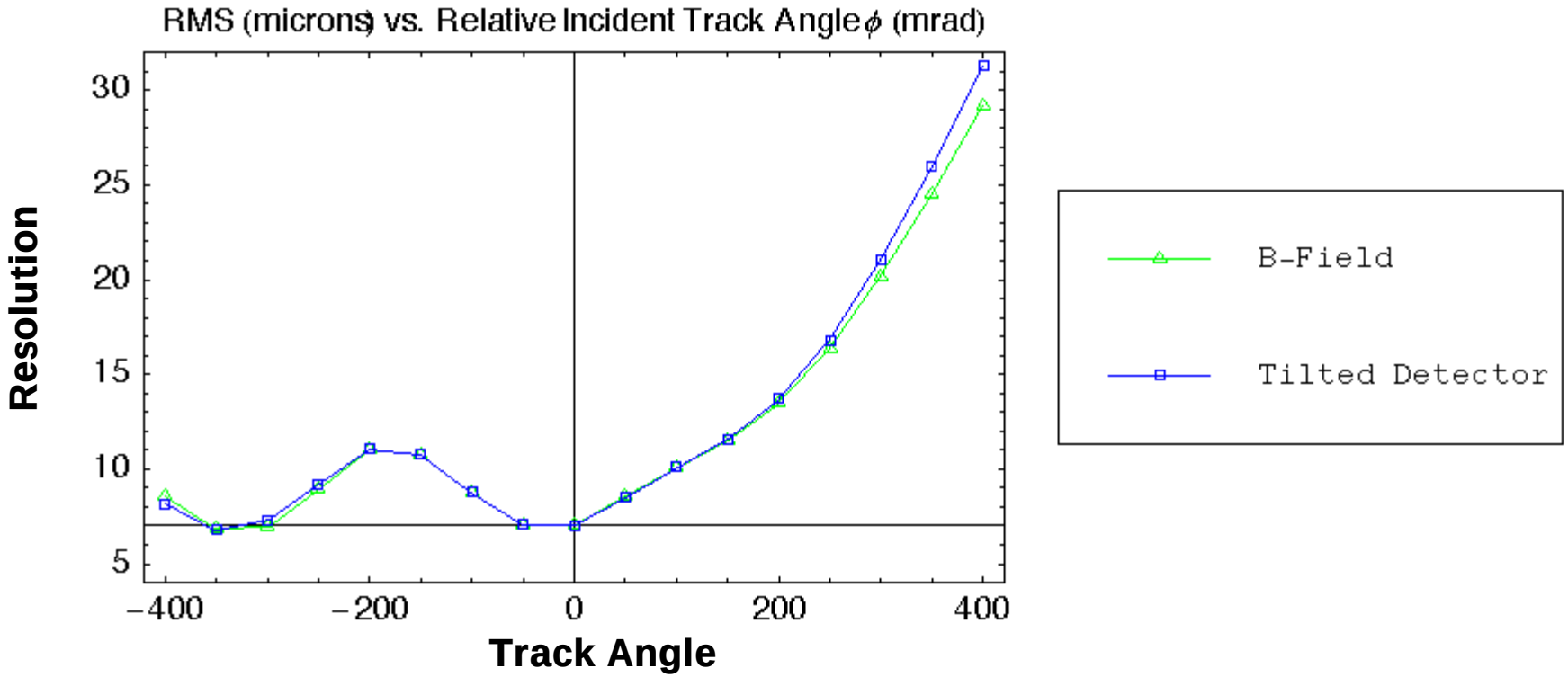


B = 5 T;
track with 200
mrad incidence

B = 0; 180 mrad tilt
track with 200
mrad incidence

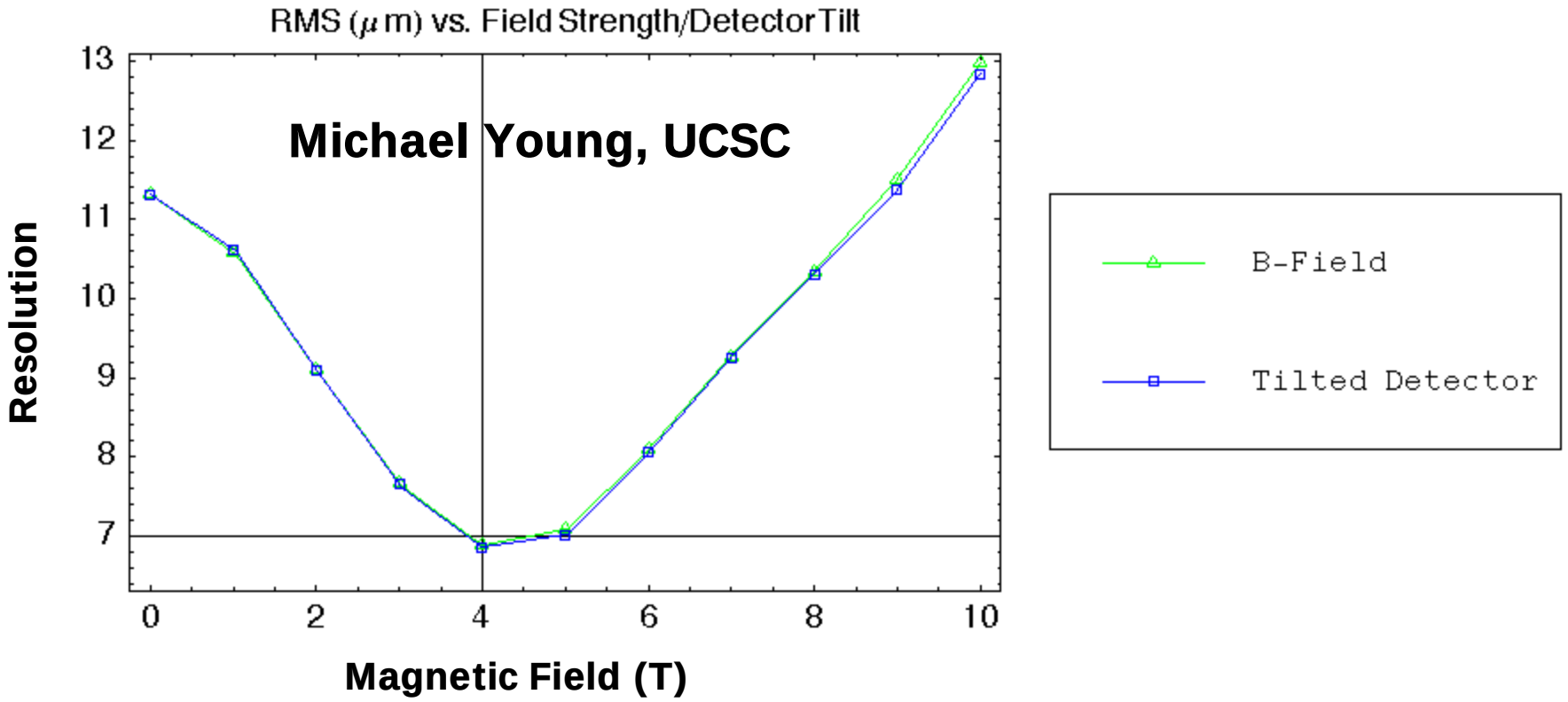
Faking the Magnetic Field

Michael Young, UCSC



Different track angles for 5T field (B-Field) or 180 mrad tilt with no B-field (Tilted).

Faking the Magnetic Field

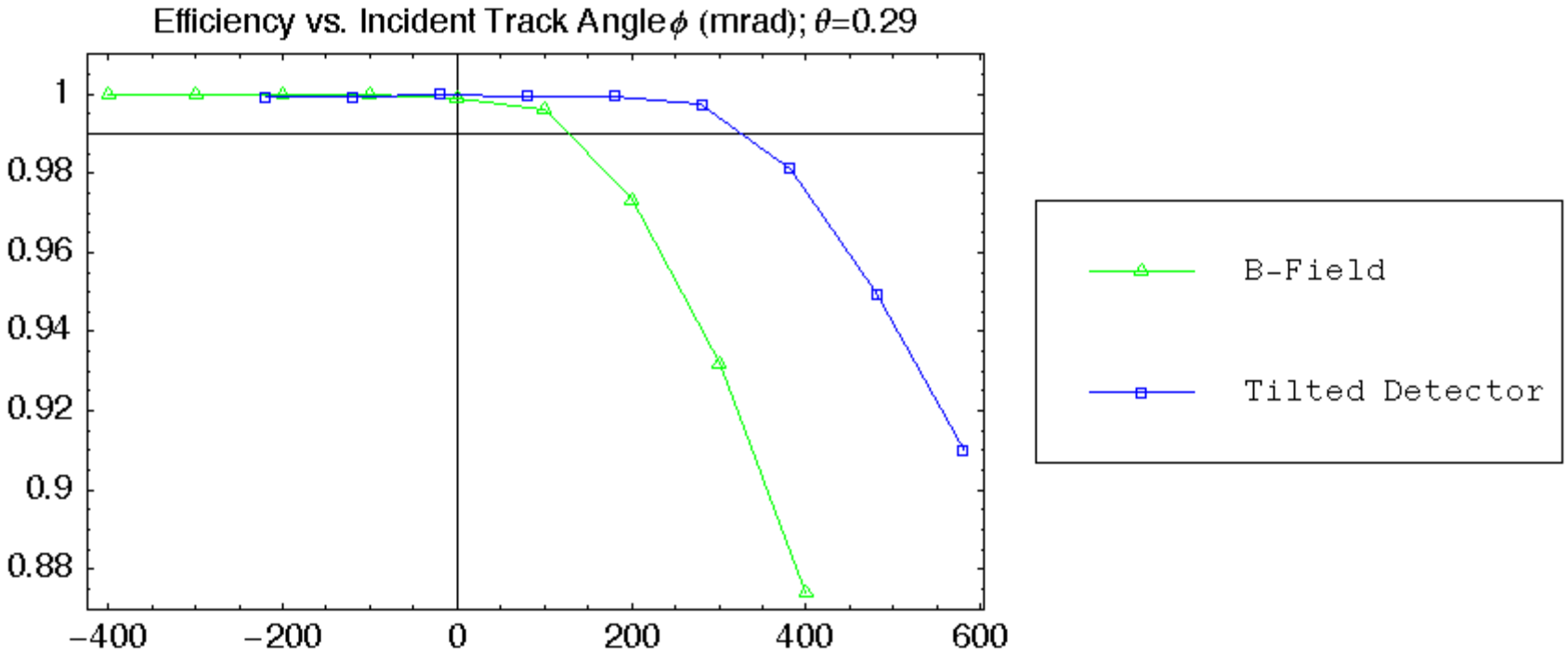


Different B-Fields (B-field) or detector tilt to simulate Lorentz angle (Tilted)

➔ Do we need high-field test beam facilities?

Efficiency versus Track Angle

Michael Young, UCSC



➔ Need to tilt detectors to regain efficiency?
(but this is for γ=10, θ=90 – worst case)

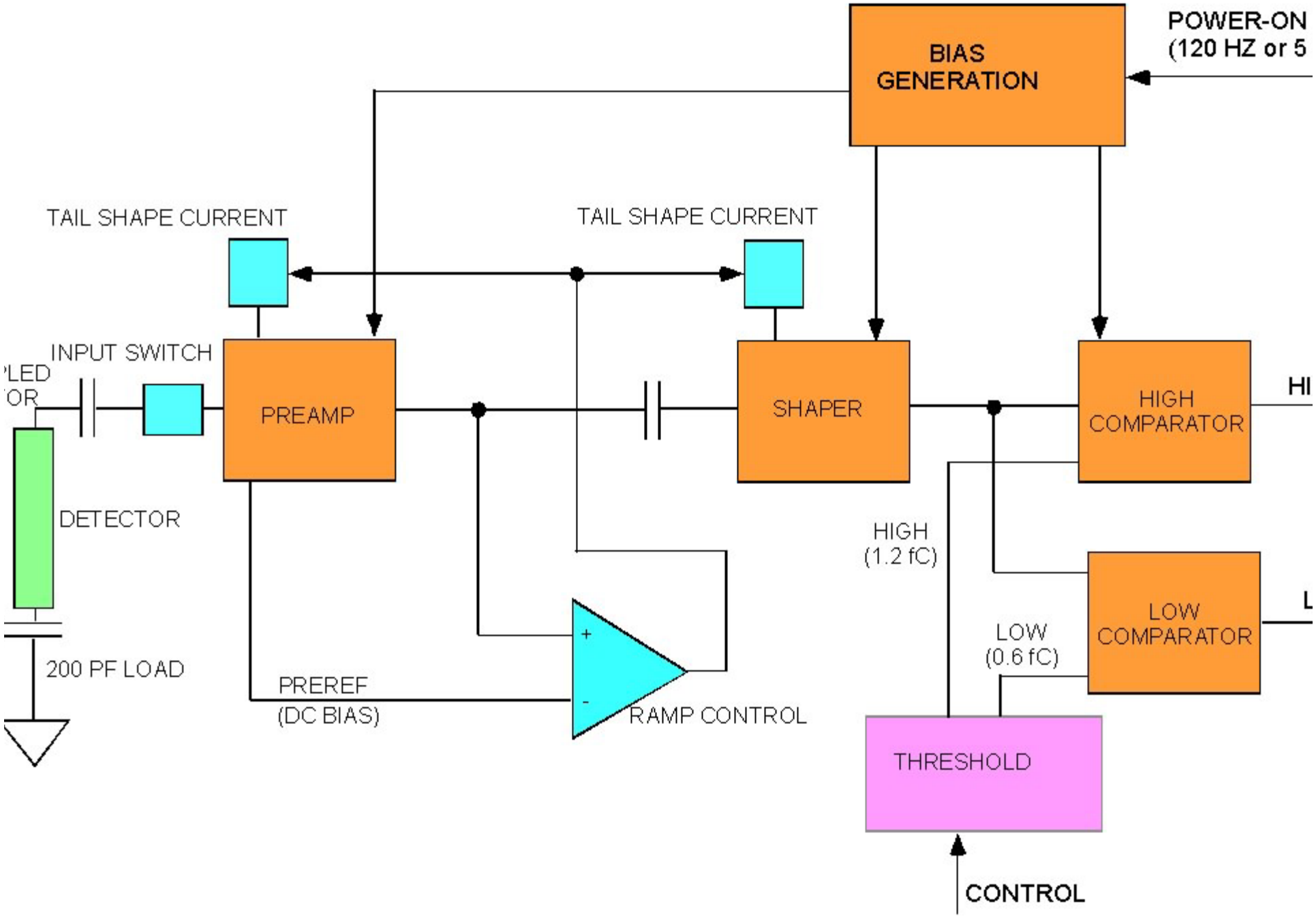
Lifestyle Choices

Based on simulation results, ASIC design will incorporate:

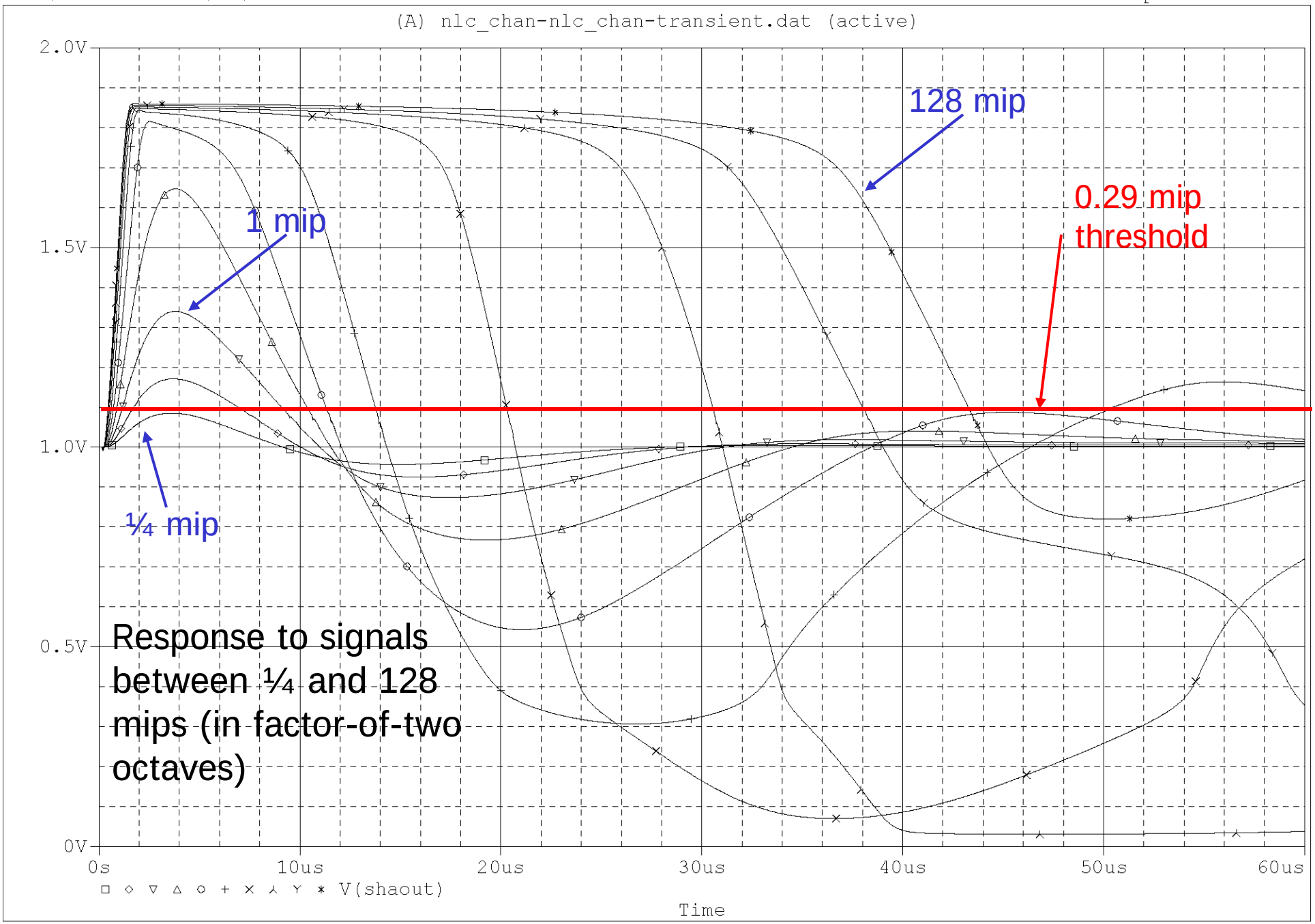
- 3 μs shaping-time for preamplifier
- Time-over-threshold analog treatment
- Dual-discriminator architecture

The design of this ASIC is now underway.

SILICON TRACKER FRONT-END ARCHITECTURE

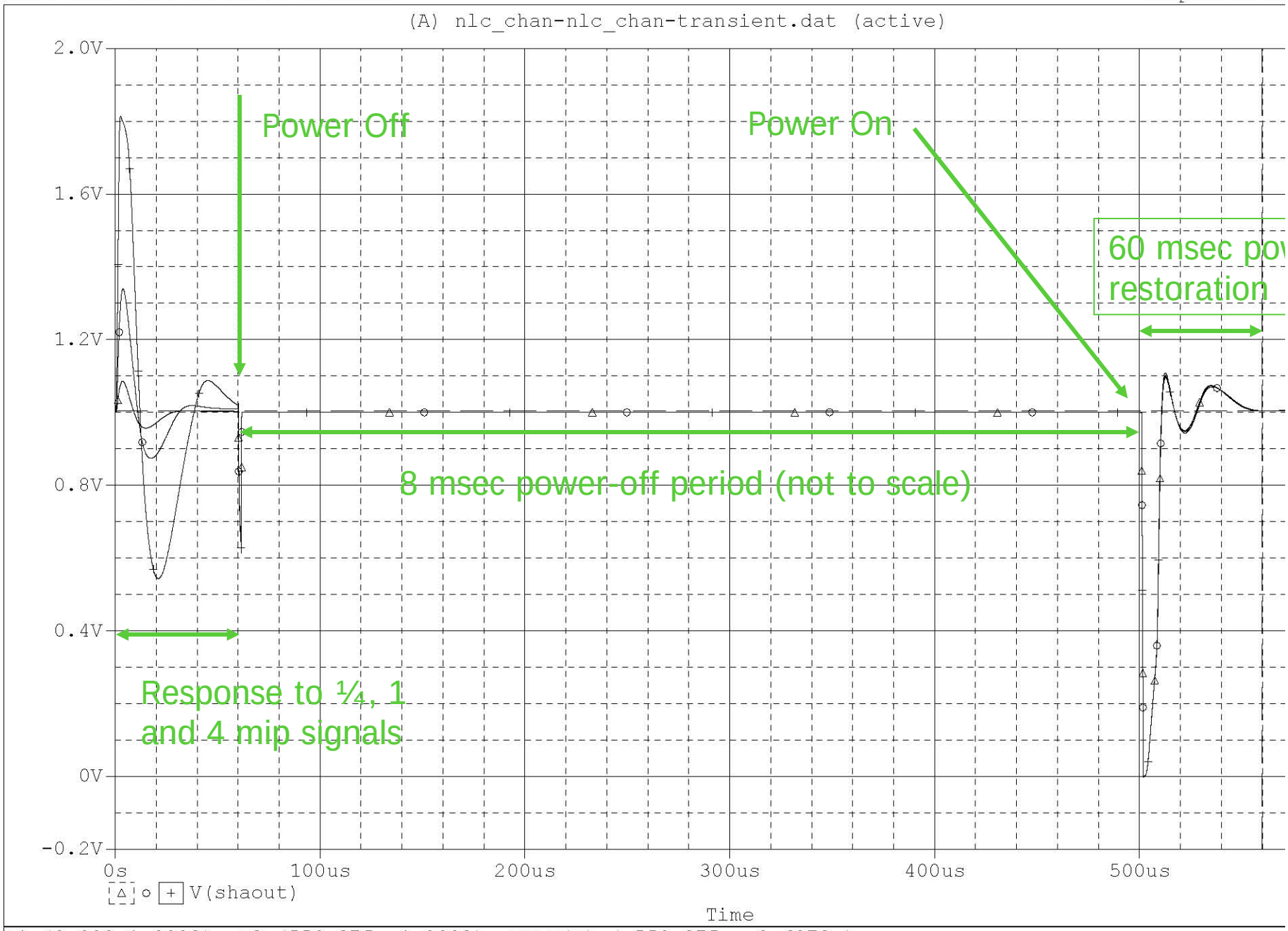


** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19 Temperature: 27.0



** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim

Date/Time run: 01/02/04 14:37:57 Temperature:



A1:(0.000,1.0002) A2:(559.875u,1.0038) DIFF(A):(-559.875u,-3.6378m)

Date: January 02, 2004 Page 1 Time: 14:

Looking ahead

Major challenges met in schematic design

Layout in specific technology (0.25 μm mixed-signal RF process from Taiwan Semiconductor) underway

Submission goal: end of August

Long ladder, Nd:YAG pulsing system, readout under development

Project is very challenging, but progress is being made, albeit slower than first envisioned.

Analog Readout Scheme: Time-Over Threshold (TOT)

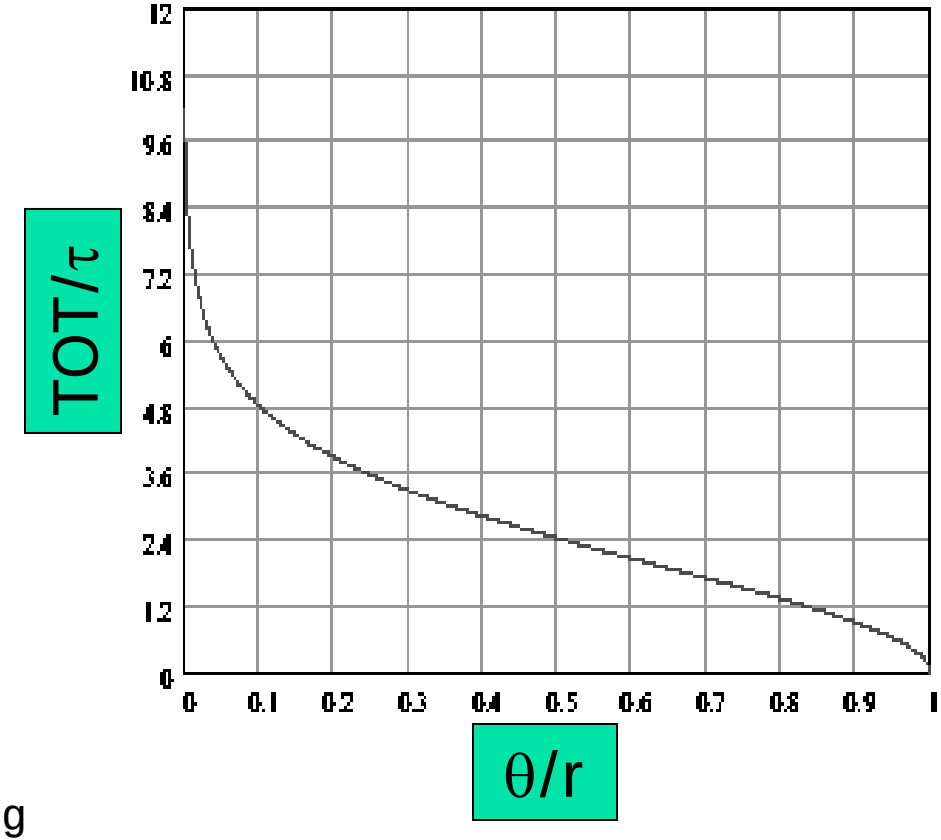
$$\theta = \frac{n_e^{\text{thresh}}}{< n_e >_{\text{min-i}}} \qquad r = \frac{n_e^{\text{pulse}}}{< n_e >_{\text{min-i}}}$$

TOT given by difference between two solutions to

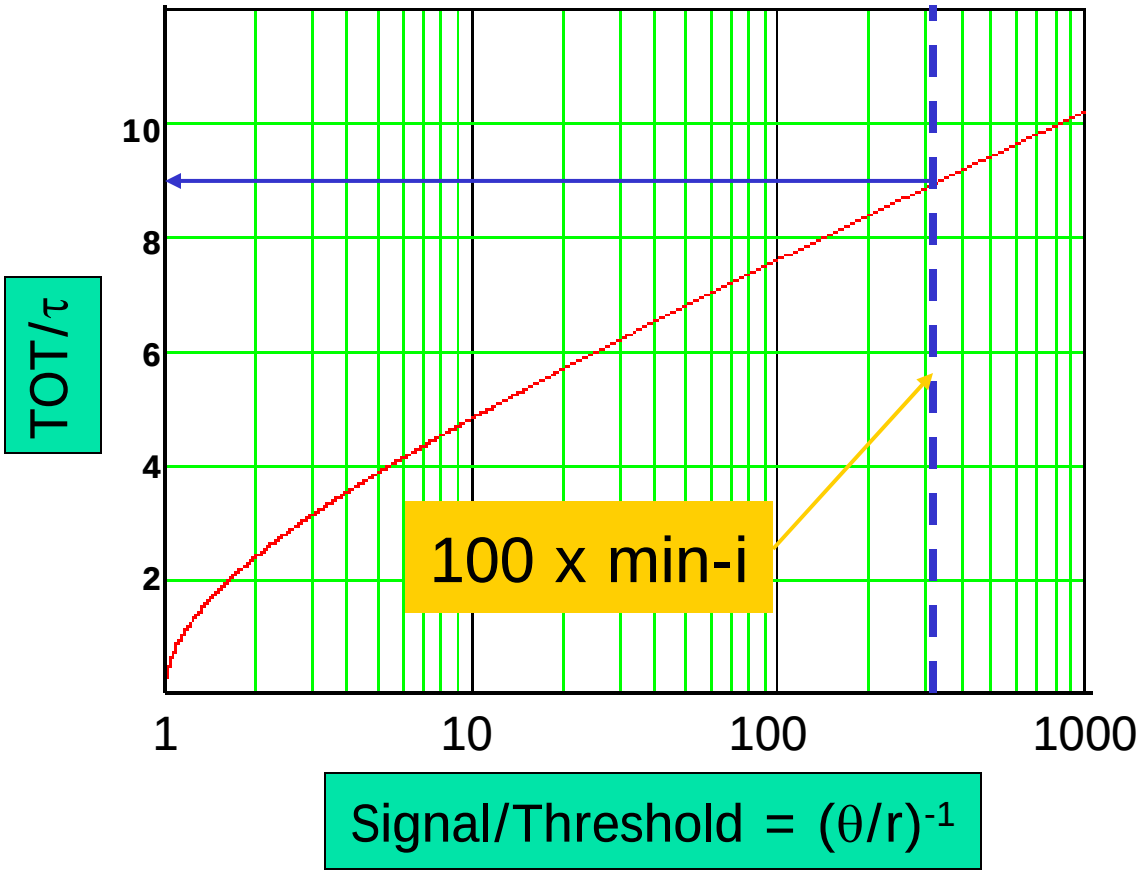
$$\frac{\theta}{r} = \frac{et}{\tau} e^{-t/\tau}$$

(RC-CR shaper)

Digitize with granularity τ/n_{dig}



Why Time-Over-Threshold?



With TOT analog readout:

Live-time for 100x dynamic range is about 9τ

With τ = 3 μs, this leads to a live-time of about 30 μs, and a duty cycle of about 1/250

➔ Sufficient for power-cycling!

Pursuing the Long-Shaping Idea

LOCAL GROUP

SCIPP/UCSC

- Optimization of readout & sensors
- Design & production of prototype ASIC
- Development of prototype ladder; testing

➔ Supported by 2-year, $95K grant from DOE Advanced Detector R&D Program