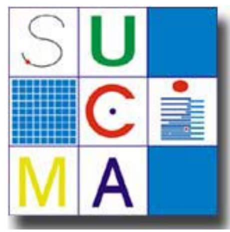

Full-size Monolithic Active Pixel Sensors in SOI Technology

- design considerations, simulations and measurements results

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on behalf of:

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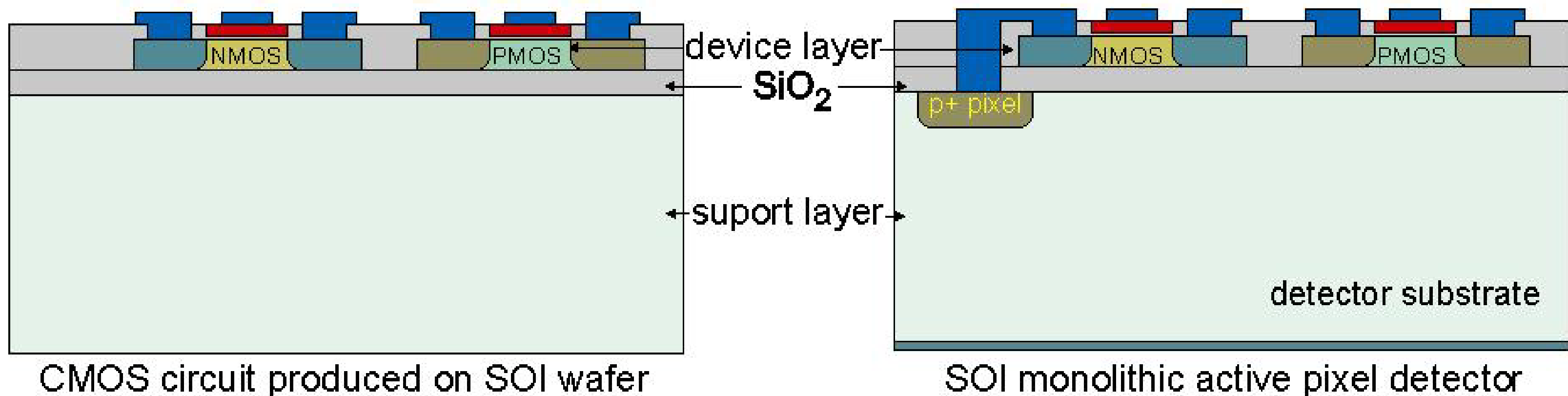
Outline

- Introduction to monolithic active pixel sensors in SOI technology
  - Basic concept of the integration of the readout electronics and particle detector using SOI wafers
  - SOI detector test structures as a preliminary validation of SOI sensor concept
- Design of the full-size SOI sensors
  - Main features of full-size SOI sensors
  - Layout optimization towards reduction of the interaction of the readout and sensitive part of the active sensor
- First measurements of full-size SOI sensors

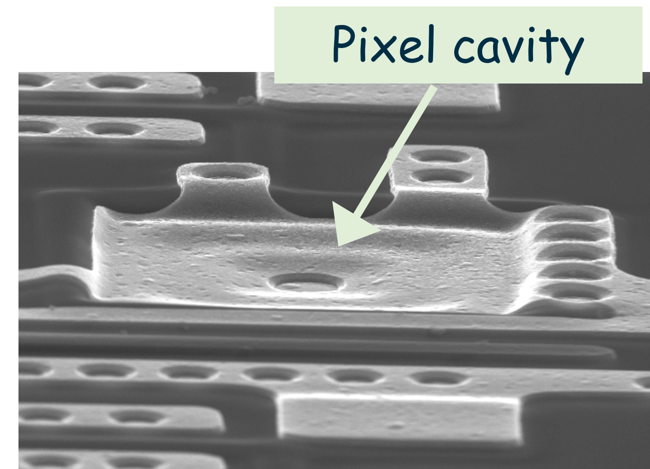
Integration of pixel detector and readout electronics in SOI technology

Basic Idea



Solution developed within SUCIMA project

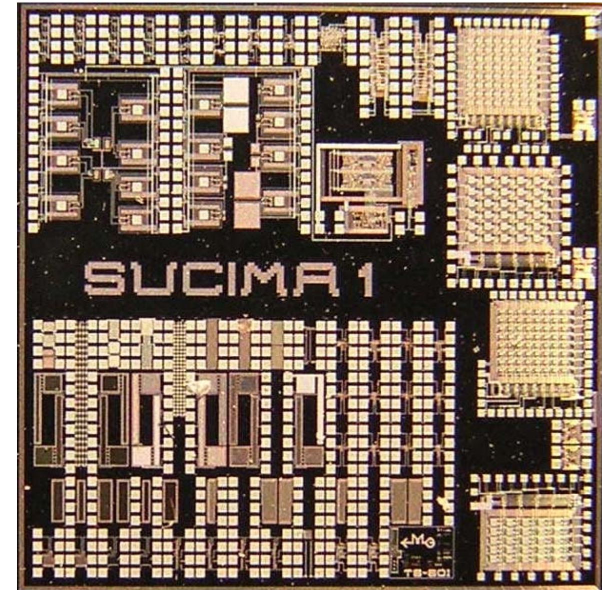
- Wafer-bonded substrates (with high resistivity support layers)
- No wafer pre-processing
- Pixel implantations created in small cavities obtained by anisotropic etching of <100> silicon
- Semi-bulk CMOS technology on thick SOI

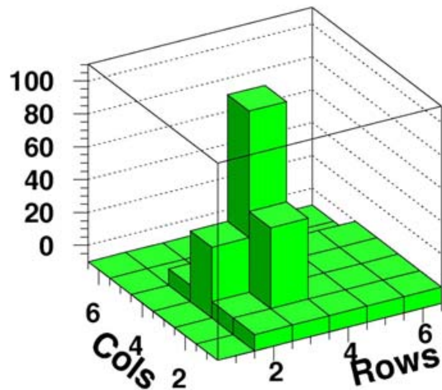


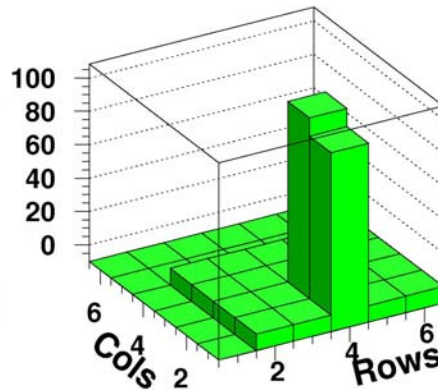
First step of development - SOI detector test structures

Basic concept of the SOI detector was first validated in several iterations of simple detector test structures:

- matrices of 8x8 sensor cells
- Cell dimensions 140x122 μm^2
- Readout channel similar to 3T cell
- No digital control blocks







Alpha particles recorded with SOI detector test structures

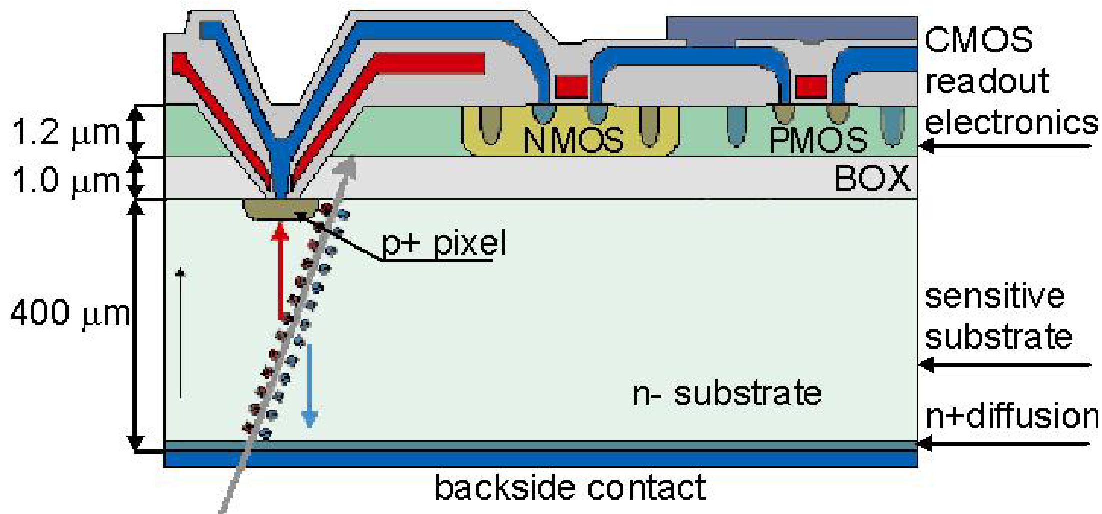
- Charge to voltage gain: 3.6 mV/fC
- Input dynamic range: 2.4 fC to 185 fC
- Leakage currents: 10 to 100 nA/cm^2

Manufacturing of full-size prototypes of SOI

- First lots of the full-size prototypes were produced on 400 μm thick SOI wafers provided by Analog Device Belfast
- Non-standard, semi-bulk technology with min feature size of 3 μm, two metal and one polySi levels was used

Device cross-section

→ the same like for the test structures



Detector substrate

- High resistive (> 4 kΩcm, FZ)
- 400 μm thick

Device layer

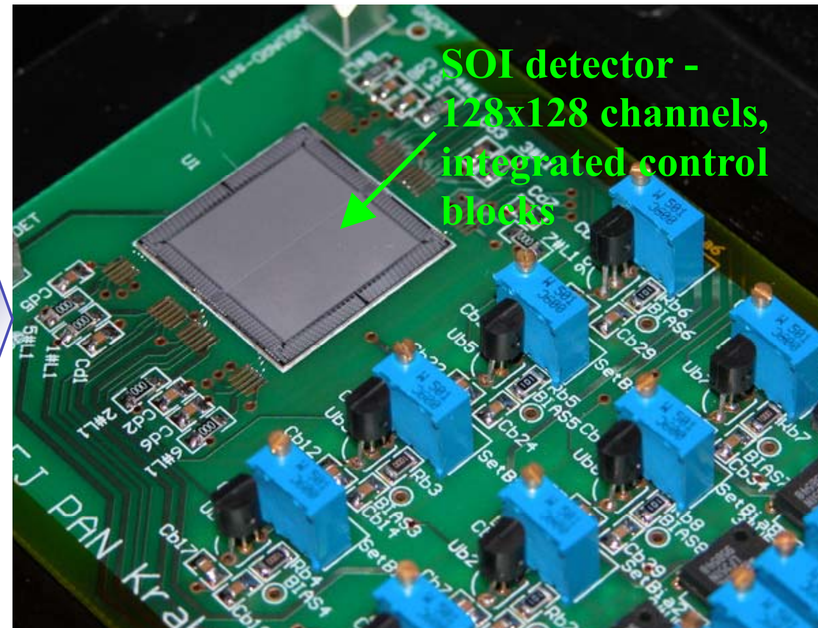
- Low resistive (9-13 Ωcm, CZ)
- 1.2 μm thick

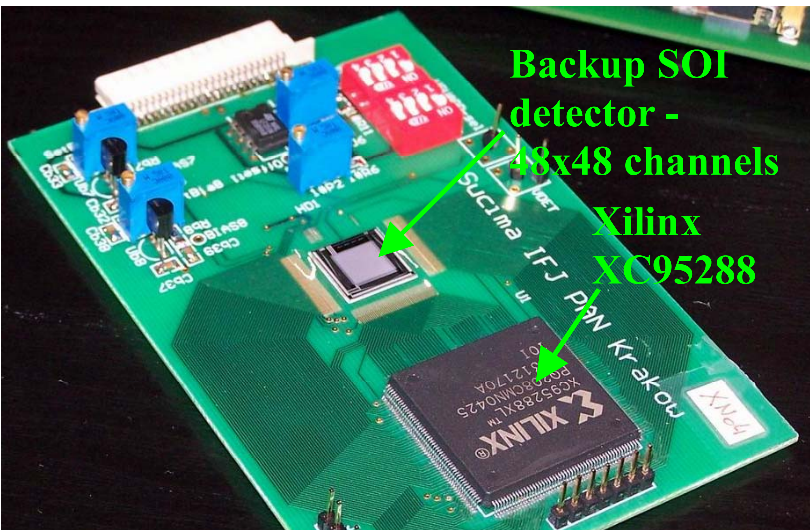
BOX

- 1.2 μm thick

Full-size SOI sensors – main features

- Fully functional detectors with implemented readout blocks on chip
  - 128 x 128 readout channels
  - area 2.4 cm x 2.4 cm
  - 4 independent sub-matrices
  - Operation in charge integration mode
  - Optimised for medical applications

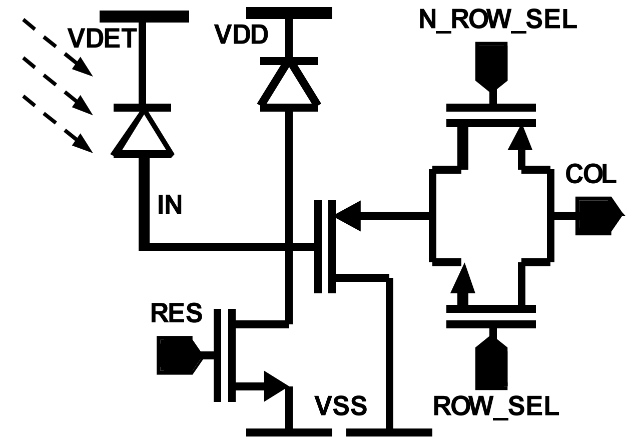


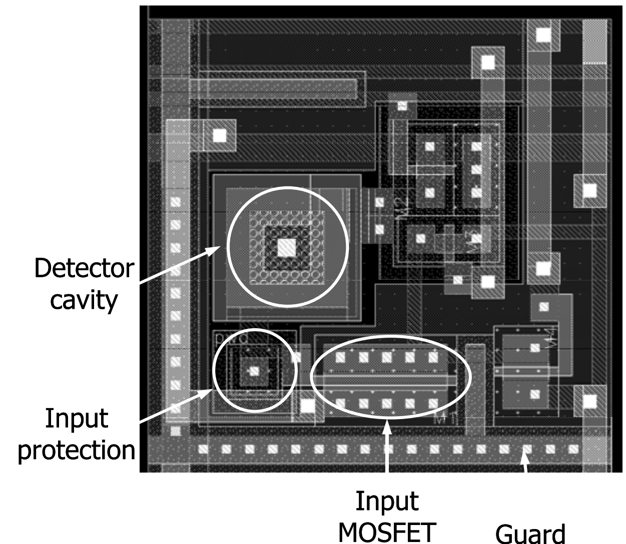


- „Baby Detector” – 48 x 48 readout channels, area 1.2 cm x 1.2 cm, no digital control blocks
- Column, row and reset signals generated by Xilinx CPLD (XC95288XL)

Full-size SOI sensors – design overview

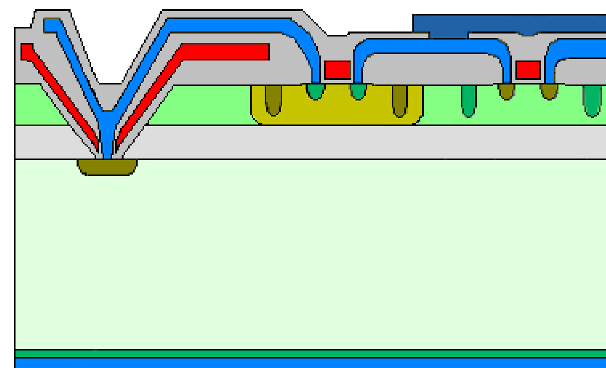
- Detector cell
  - Dimensions 150x150 μm^2
  - Similar to 3T cell, but consists of both transistor types
- Readout
  - Serial, analogue output (for larger prototypes 4 parallel outputs)
  - Double sampling for external CDS
  - Sensor dead-time below 1% with respect to integration time
- Basic parameters according to design
  - Dynamic range: up to 500 fC (but may be limited by leakage current)
  - Charge to voltage gain: 3.6 mV/fC
  - Readout frequency: up to 4 MHz





Sensor optimisation from the point of view of the interaction between detector and readout part

- In MAPS sensors the detector sensitive part and the readout electronics are manufactured in direct proximity ⇒ interaction of these two parts has to taken into account during sensor design.



- Two effects has to be investigated
  - Influence of the biasing of the electronics of the potential distribution in the detector substrate
  - Crosstalk between electronics and detector substrate
- In some earlier developments special shielding structure was proposed to over come the problems of the interaction of the detector and electronics – complicated technology and wafer pre-processing is required. We want to avoid additional technological steps.

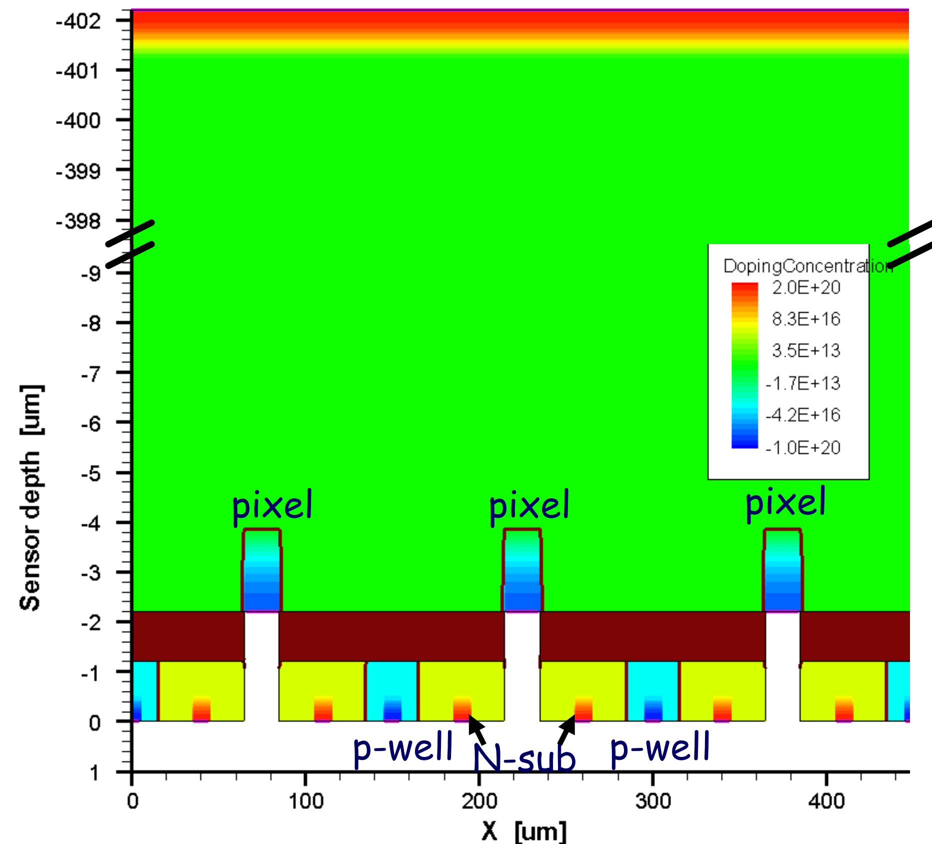
Simulations of electrostatic potential distribution in the detector substrate

How can the electronics influence detector operation?

- Sensor configuration – small pixel implantations (25 μm wide). Over gaps between them electronics is operating.
- Source/drain implantations - far from BOX interface, electronics substrate is biased ⇒ voltage applied to S/D should not affect significantly the potential distribution in the detector.
- But voltage applied to the electronics substrate and wells may be important.
- Especially dangerous areas below P-wells – they may reach BOX and are connected to the lowest potential in the circuit ⇒ may cause local potential minima, which may disturb the collection of the charge generated underneath.

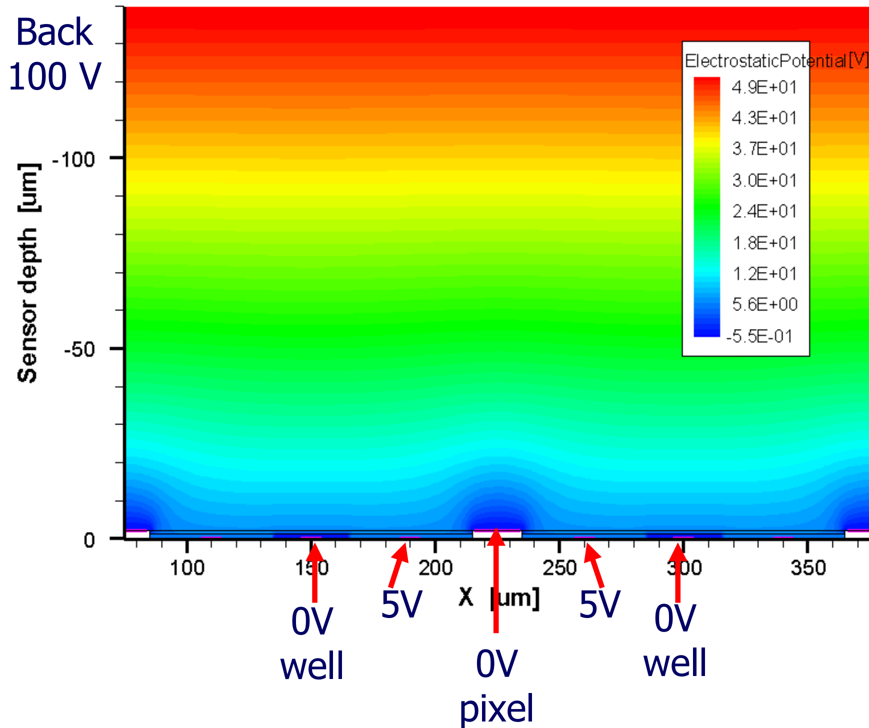
Simulations performed with ISE-TCAD

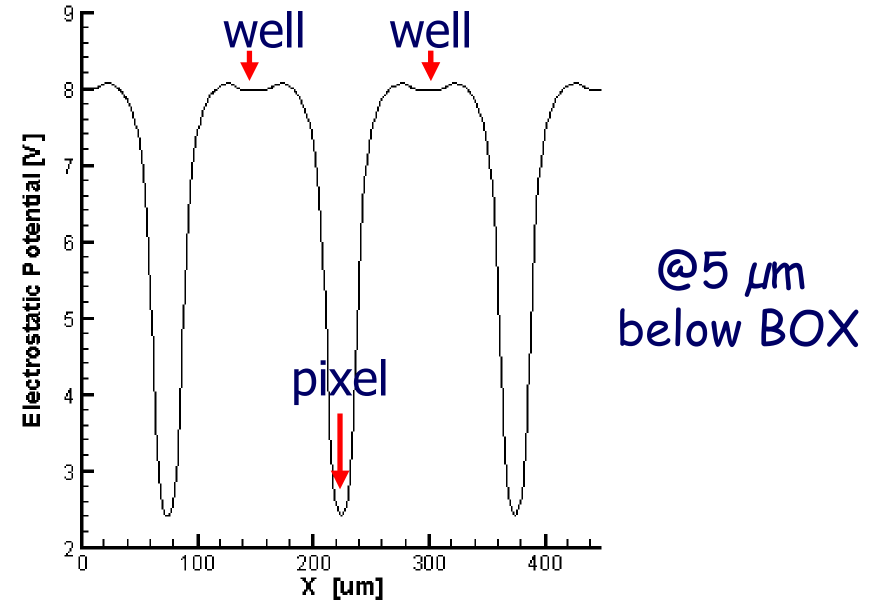
Simulated model



Simulations of electrostatic potential distribution in the detector substrate

Potential distribution for basic SOI sensor structure



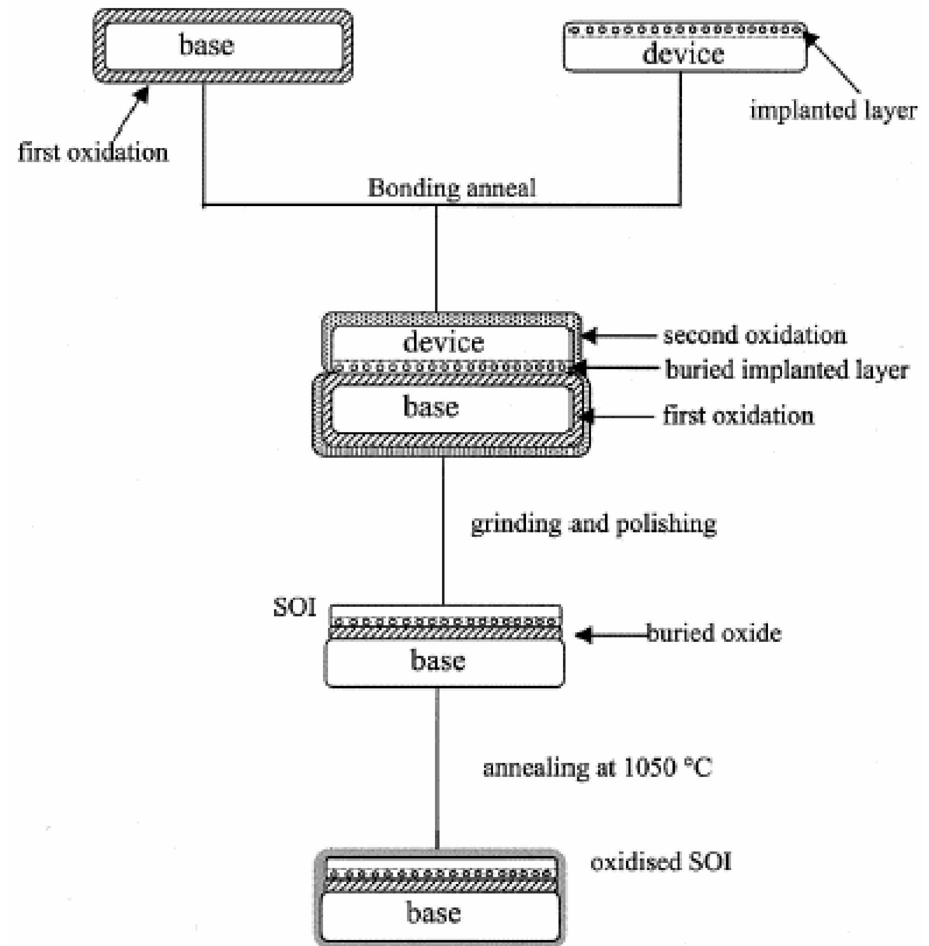


@5 μm below BOX

- For basic SOI sensor structure distortion of electric field may be observed
- The effect on the detector operation will strongly depend on the sensor cell layout and well profile (if it reaches BOX)

Simulations of electrostatic potential distribution in the detector substrate

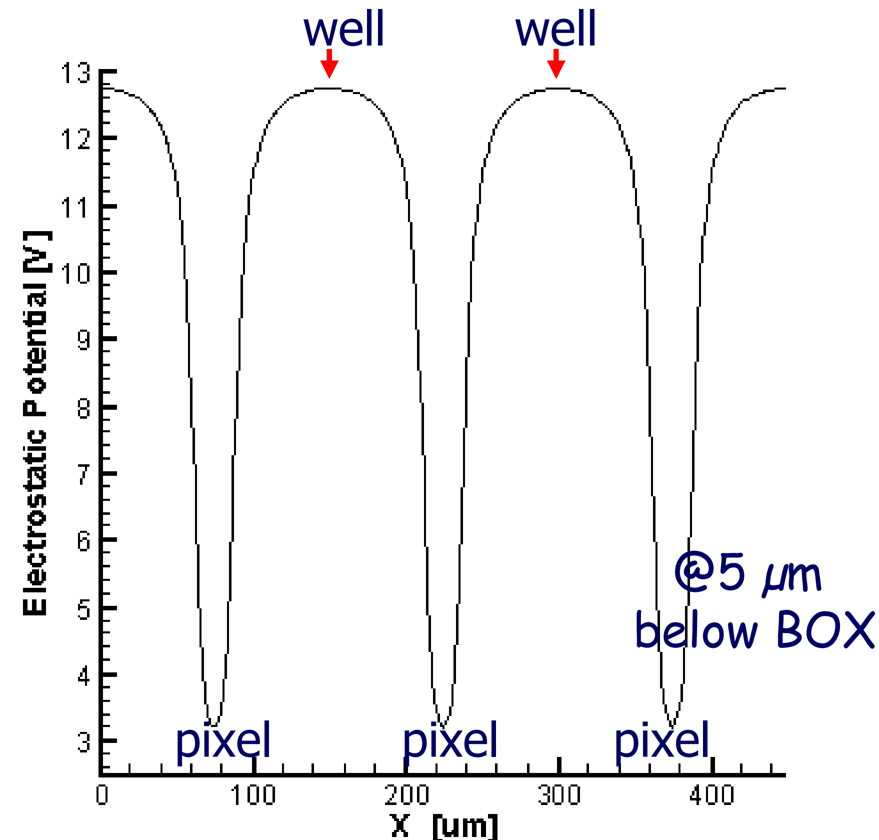
- Solution of the problem – without changing the sensor layout or the technology – usage of wafers with a buried implanted layer (blanket).
- Blanket - shallow, highly doped region at the interface between the device layer and BOX; used for impurities gettering in silicon film.
- In SOI sensor buried implanted layer may play the role of a shield.



Simulations of electrostatic potential distribution in the detector substrate

- IceMos Technology – one of the suppliers of the SOI wafers for the SOI project – provides SOI wafers with customized buried implanted layers – it is a standard option.
- First batch of the full-size SOI sensors was produced on wafers without blanket, but for future production buried implanted layers are going to be used.
- The implantation dose and energy will have to optimised to form efficient shielding without changing electronics performance.

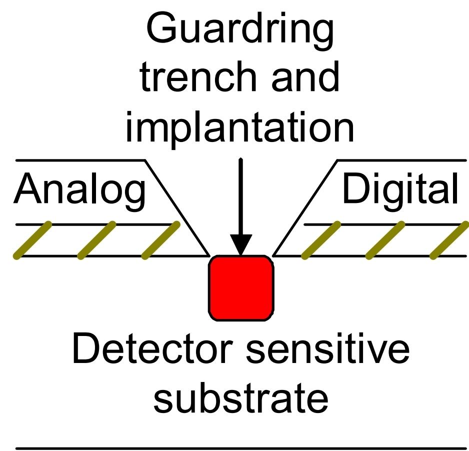
Potential distribution for SOI sensor structure with shallow buried implanted layer - arsenic with top concentration of $10^{18}/cm^3$



Electronics–detector substrate crosstalk

- Sudden changes of the voltage signal levels in the front-end electronics may cause injection of parasitic current signals into the detector substrate through the BOX.
- Possible source of such interferences in SOI sensors:
  - digital part of the chip – it becomes important for full-size prototypes
  - the steering lines of the readout cells
  - these electrodes of the transistors in readout cells on which the potential may suddenly change during the circuit operation
- To minimize the crosstalk, the layout of the prototypes of the sensor had to be optimized. Remaining interferences can be subtracted as a systematic noise.

Reducing interferences from digital part



From row/column selection lines

Electronics–detector substrate crosstalk

Reducing interferences from remaining steering lines – resent line

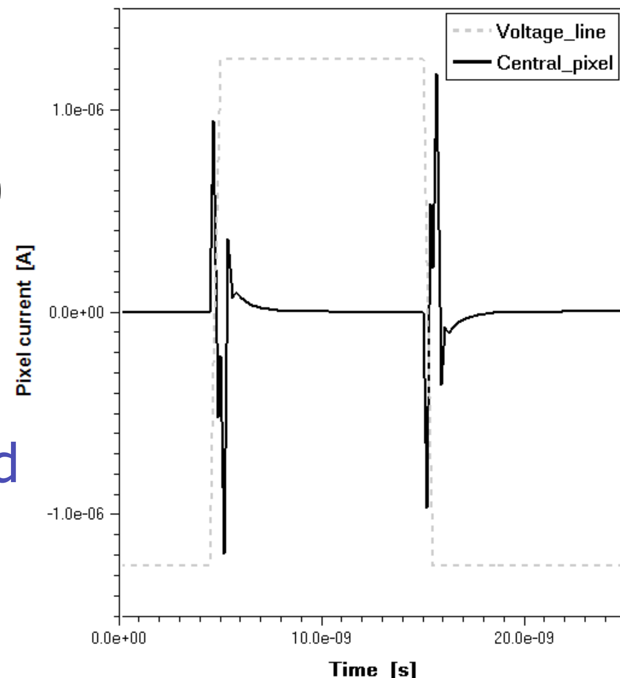
- Substrate densely grounded along the reset line – on the layout of the chip substrate contact and line are at the distance of 4.5 μm
- In the proposed solution of the SOI sensor thick device layer and BOX are used, which should also allow reduce crosstalk
- To investigate the effectiveness of this approach mixed-mode simulations were performed with ISE-TCAD

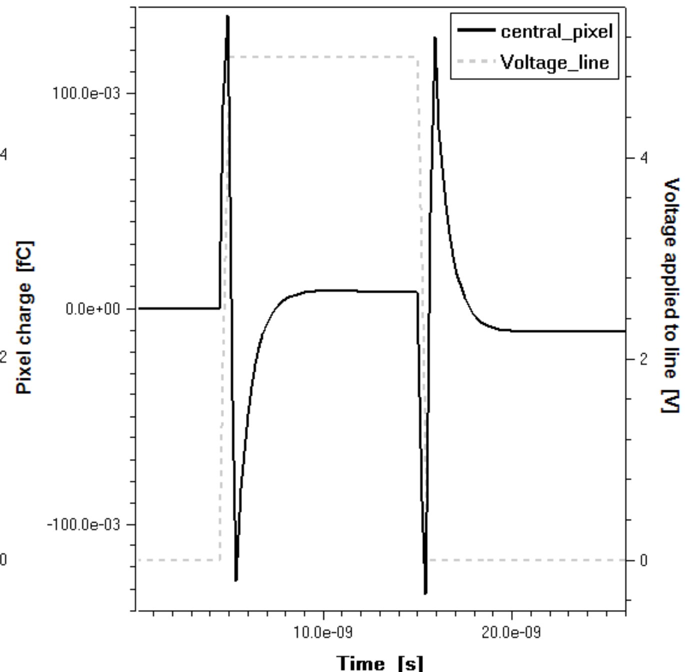
Analysed model:

150 μm long line

at the distance of 10 μm from substrate contact and 40 μm from pixel

In terms of integrated charge negligible crosstalk observed.



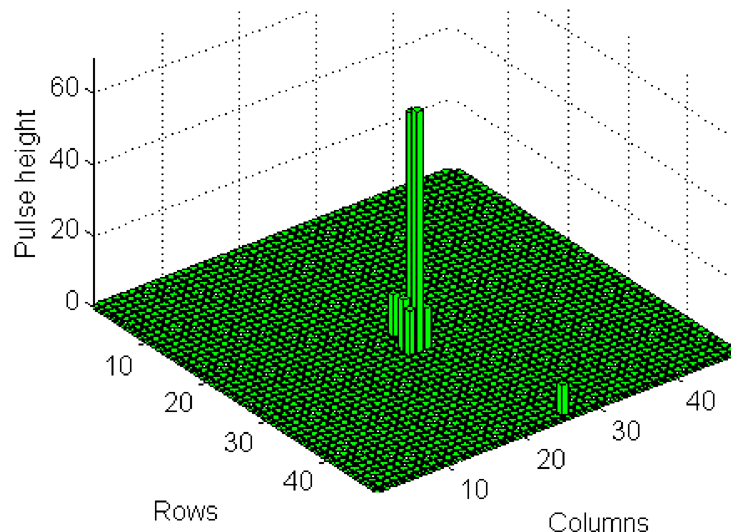


Full-size SOI sensors – first tests

- One batch (3 lots) of full size SOI sensors was produced. Chips from one lot tested – six larger and 4 smaller sensors.
- Problems with the production yield – for the best of large sensor proper readout operation observed for 3 quarters, one of smaller sensor has relatively good performance
- Very preliminary test results:
  - Senor sensitivity observed with laser pointer and α particles
  - Readout frequency up to 4 MHz, digital part tested up to 10 MHz without any problems

Recorded α particle

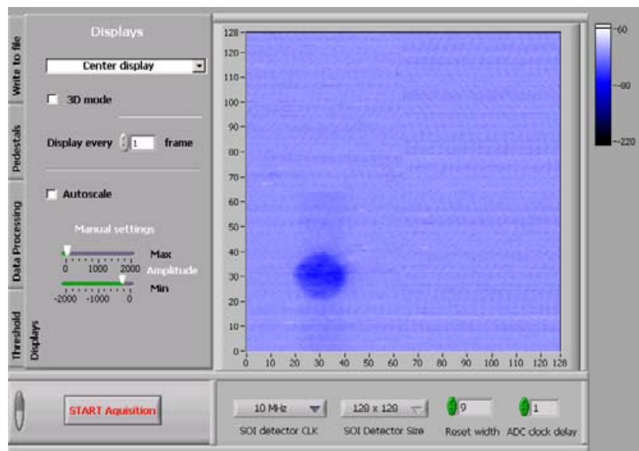
Detector: 48x48 cells

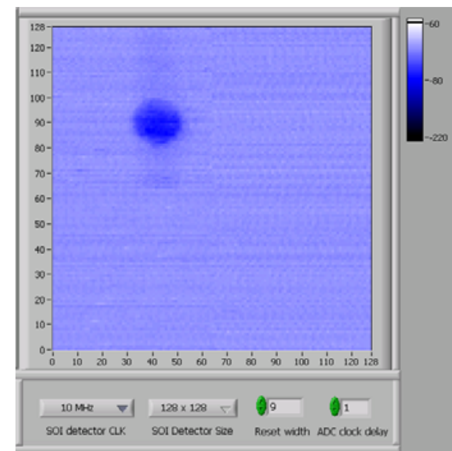


Visualization of the readout results

Detector: 128x128 cells

Laser pointer light shined on two different quarters of the detector

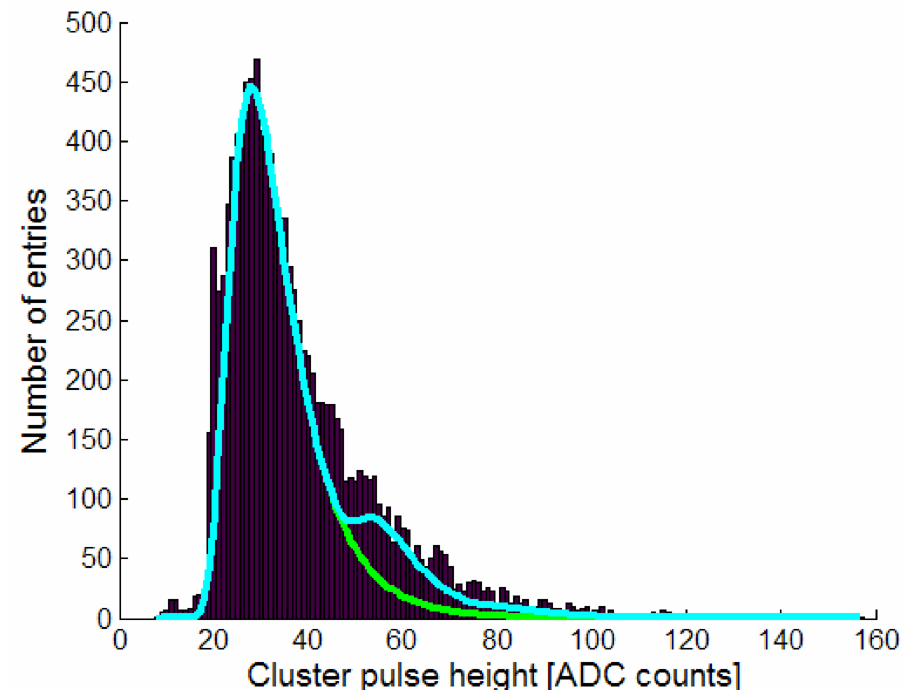




Full-size SOI sensors – first tests (cont.)

- MIP response was measured with „baby detector" (48x48 chan.)
- Tests performed with Sr90 source
- Sensor connected to SUCIMA imager DAQ system
- V_{DET}=115 V, t_{int}=2.3 ms
- Noise per pixel: 1.7 to 2.5 ADC
- Most probably cluster height: 28 ADC (corresponding to 14 mV)
- Due to long integration time signal corresponding to more than one detected particle are visible.

Measured distribution of beta particles from ^{90}Sr source. Green line -Landau fit corresponding to a single MIP particle; blue line - sum of Landau fits corresponding to up to 3 MIP particles recorded during integration time.



Summary

- First full-size MAPS in SOI technology were designed and produced.
- For the new sensors the methods of the reduction of the interaction between the readout and the radiation sensitive parts of the active sensor were investigated:
  - Use of the SOI wafers with n+ buried implanted layers was proposed as an efficient method of shielding the readout circuitry form the detector substrate.
  - Dense device layer polarization and usage of parallel steering lines was suggested for the reduction of the electronics-detector crosstalk.
- First tests of full-size indicated some problems with production yield. The possible reason are observed variation of device layer thickness (of order of 200%) related to the thinning down method use by wafers supplier.
- For good structures proper readout operation and sensitivity to ionising radiation was observed.
- MIP signal was measured - obtained cluster height in good agreement with predicted charge to voltage gain.
- Directions of further development:
  - Thanks to the kindness of the DEPFET group from Bonn we have next sensors assembled – the performance and reliability of these sensors will be investigated.
  - For the next batches of sensors the layout of the pixel cavity will be improve to obtain better reliability of the sensors.
  - Interaction of the readout electronics and the detector substrate, as one of the most specific aspect of the SOI implementation, will have to be investigated experimentally.