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Development of monolithic active pixel detector in SOI technology

W. Kucewicz[a,*], A. Bulgheroni[b], M. Caccia[b], P. Grabiec[c], J. Marczewski[c], H. Niemiec[a]

[a]*Department of Electronics, AGH-University of Science and Technology, Al. Mickiewicza 30, 30-059 Krakow, Poland*
[b]*Universita dell Insubria, via Valleggio 11, 22100 Como, Italy*
[c]*Institute of Electron Technology, Al. Lotnikow 32/46, 02-668 Warsaw, Poland*

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Abstract

A novel solution of an active pixel detector, which exploits wafer-bonded Silicon on Insulator (SOI) substrates for integration of the readout electronics with the pixel detector, is presented. The main concepts of the proposed monolithic sensor and the preliminary tests results with ionising radiation sources are addressed.

SOI is an alternative solution of a monolithic active pixel detector, which allows integrating fully depleted sensor and front-end electronics active layers into one silicon wafer. The main idea of the sensor relies on the use of both the monolithic silicon layers (device and support layers) of the SOI substrate for fabrication of pixel detector diodes and readout electronics.

Such detectors can find a wide range of applications, not only in particle physics but also in medicine, space science and many other disciplines.

The sensor structure and the readout configuration have been developed and the measurements of a dedicated test structure have validated the new technology of the SOI detector. Then small SOI sensor matrices with 8×8 channels have been recently produced and tested.

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Keywords: Silicon detector; Active pixel detector; SOI technology

1. Introduction

Progress in the fabrication methods of Silicon on Insulator (SOI) substrates, especially a new technique called wafer bonding, was the motivation for an idea of a novel monolithic active pixel

*Corresponding author. Tel.: +48 12 617 30 45; fax: +48 12 633 23 98.
E-mail address: kucewicz@agh.edu.pl (W. Kucewicz).

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detector realized in SOI technology. An important advantage of the wafer-bonded substrates in comparison with other popular SOI substrates obtained in the SIMOX process is the lower level of structural defects in both device and support layer and the absence of silicon inclusions and islands in the buried oxide [1]. The construction of the sensor relies on the utilization of both the silicon layers (device and support layers) of the SOI substrate.

As presented in Fig. 1, the sensor part is realized in the SOI high-resistivity ($>4\,k\Omega\,cm$) support layer and acts as a particle detector. The sensor is 300 μm thick and it has a conventional form of a matrix of p+–n junctions. Similar to the standard hybrid pixel sensors, it may operate in full depletion in order to achieve high detection efficiency.

The readout electronics is fabricated in the low-resistive, 1.5 μm thick device layer and it is monolithically coupled with the detector by a connection that passes through the buried oxide. Since the buried oxide separates the detector and the electronics active layers, transistors of both types may be used in the readout circuitry thereby increasing the flexibility of the design.

With respect to the hybrid pixel solution, the SOI sensor as a monolithic device allows reducing the total sensor thickness and eliminates the complicated bump-bonding process. On the other hand, the SOI solution, exploiting high-resistive detector substrates as sensitive layers, allows achieving higher detection efficiency with respect to CMOS detectors. The use of wafer-bonded SOI substrate allows optimisation of the resistivity of the electronics and detector layers.

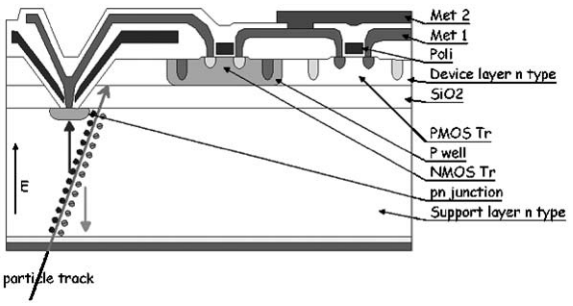

Fig. 1. Cross section of the SOI pixel sensor.

In the presented solution, commercially available SOI substrates are used since both the readout electronics and detector diodes are created after the bonding process and no wafer pre-processing is required.

The SOI sensor project was started in 2001 and is partially supported by the European Commission within the Fifth Framework Program called SUCIMA (Silicon Ultra Fast Camera for Gamma and Beta Sources in Medical Applications). One of its goals is the development of a monolithic sensor optimised for medical imaging applications, especially dosimetry of radioactive sources for brachytherapy and beam monitoring for hadron therapy [2].

2. SOI technology validation

The SOI sensor described above required the development and validation of a new non-standard technology, which allows the creation of a connection between the electronics and the detector layers as well as fabrication of the devices at both sides of the buried oxide. For this reason, a special technological sequence that consists of more than 100 individual processes was defined at the Institute of Electron Technology in Warsaw [3]. For technology characterization and validation, a dedicated test structure was designed and fabricated. This test structure includes several units, such as general technological test structures (for parameters extraction, investigation of device mismatches, reliability tests, etc.) and specific structures for SOI detector applications [4].

Since the readout circuits for the silicon pixel detectors are made by matrices of the readout channels that should have very similar parameters, special effort was also made to investigate the parameter mismatches of the typical elements of electronic circuits. Satisfactory parameter uniformity was obtained for the investigated elements [5].

3. Small area SOI detector

In order to examine the functionality of the SOI active pixel sensor, small matrices of 8×8 diodes with associated DC coupled readout channels (Fig. 2) were designed on the SOI test structures. Every readout channel of these matrices has configuration similar to the three transistors (3T) cell [6], widely used in the CMOS imagers. Taking advantage of the separation of the detector and electronics active layers in the SOI sensors, some modifications of the basic 3T readout cell were made in the design. The one-transistor channel selection switches were replaced by transmission gates to obtain better linearity and dynamic range, and the reset transistors of the opposite type than the input transistors were used to achieve faster discharging of integrating capacitances. Since the SOI solution provides a possibility to polarize the detector pixels with high voltages, each pixel has also incorporated a special diode in order to protect the readout channel input. It switches on when the input voltage exceeds the supply voltage of the electronics. The contribution of this diode to the total sensor leakage current proved to be negligible with respect to high voltage bias of the sensor diodes. A basic cell, presented in Fig. 2, consists of the following elements: input transistor acting as a source follower, resetting transistor, which periodically discharges integration capacitance of the detector, and row-selection transmission gate.

The proposed configuration of the readout channel was strictly linked to SUCIMA applications [2]. The charge generated in the sensitive volume is integrated on the pixel capacitance during a given time period. The dimensions of the single cell are $140 \times 122\,\mu m^2$.

The concept of the SOI detector was validated in several sets of measurements of the SOI detector test structures, which were fabricated in many iterations at the Institute of Electron Technology in Warsaw. The parameters of the stand-alone readout electronics and the pixel diodes as well as the performance of the complete sensors were examined. The measurements were performed for the bare sensor chip, in order to investigate the detector dynamic range and linearity, and for the sensor connected to the advanced data acquisition system called SUCIMA Imager [7], developed for the above-mentioned European Project [2].

The readout method of front-end circuit is based on classical serial analogue organisation. The analogue readout allows increasing single-point resolution of the sensor by the measurement of signals on neighbouring channels and proper interpolation. In order to obtain a high quality of imaging also, a well-defined integration time for every channel is required. For this reason a special novel readout sequence was developed. This solution is in principle similar to the rolling shutter technique [8], where the rows of the readout matrix are both reset and read out (after integration time) one by one in the same sequence and at the same speed. In contrast to this traditional technique, during the proposed readout sequence every channel can be accessed twice: immediately after reset of diode and after integration time, which is equal to the readout time of the whole matrix. This method not only guarantees very short detector

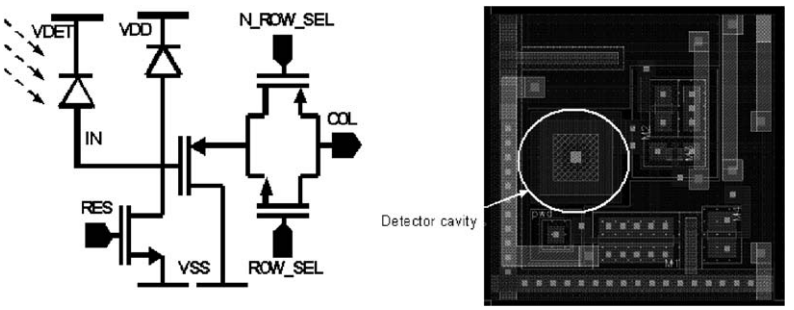

Fig. 2. Schematic view and layout of the prototype SOI sensor cell.

dead time (limited to the reset time of integrating element) and well-defined and adjustable integration time, but also enables external correlated double sampling (CDS) processing that ensures kTC and fixed pattern noises suppression.

The sensor sensitivity for ionising radiation and the linearity of the readout response were preliminarily tested with an infrared laser spot (with a wavelength of 850 nm). During the integration time of 1 ms, different numbers of 4 μs wide light pulses were injected and for every number of the light pulse 10 000 events were recorded and the results averaged. The measured values of output signals (after correlated double sampling (CDS) processing and pedestal subtraction) versus input charge are illustrated in Fig. 3. The linear response as a function of the generated charge in the investigated range up to 45 MIPs can be clearly observed.

Further tests of the small area SOI detectors were performed with the ^{90}Sr beta source. The energy spectrum of the source was measured using the SUCIMA-Imager DAQ system with an integration time of 720 μs and a fully depleted detector. The obtained histogram after cluster calculation is presented in Fig. 4. As expected, a Landau distribution of the signals was obtained and the most probable value of 27 ADC counts corresponding to the MIP signal was measured. These results prove the sensitivity of the test matrices for the MIP signals and the effectiveness of the charge integration mechanism implemented in the readout circuit.

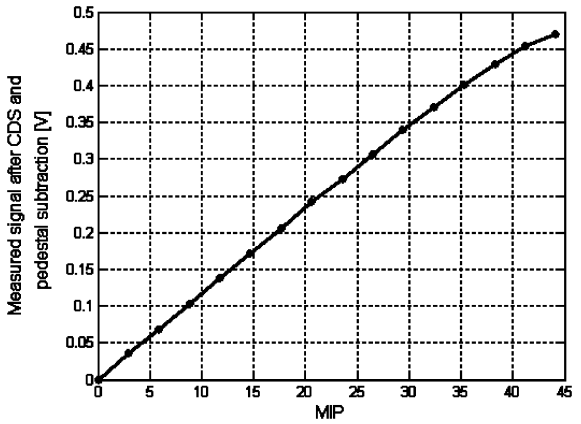

Fig. 3. Output signal from the test structures of the SOI sensor versus injected charge in MIP units.

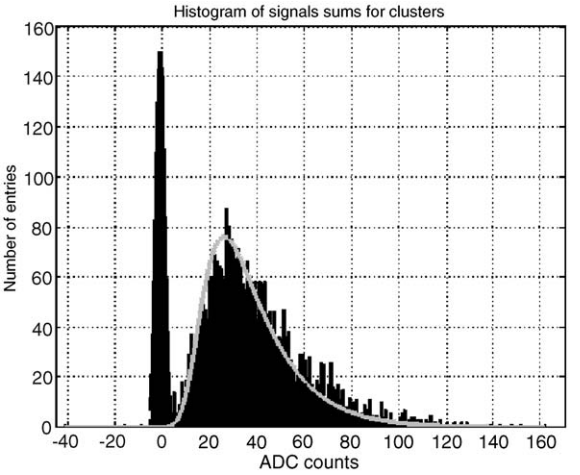

Fig. 4. The signal spectra obtained with SOI sensor test structures for ^{90}Sr radioactive source. Grey histogram and line indicate pedestal and its Gaussian fit, black histogram and line indicate the signal from ^{90}Sr beta source and its Landau fit.

4. Full-scale detector

After promising results of measurement of small-area detector, the full-scale detector was designed and sent to production. It is a completely functional sensor with the digital control blocks supervising readout operation implemented on the chip. The layout of the sensor is presented in Fig. 5. The chip (with total dimensions of $24 \times 24\,\text{mm}^2$) covers the active area of $19.2 \times 19.2\,\text{mm}^2$ and it consists of 16 384 channels. The single cell dimensions are $150 \times 150\,\mu\text{m}^2$. The detector consists of four functionally independent sub-segments with dimensions of $12 \times 12\,\text{mm}^2$ and 64×64 readout channels each. Every sub-segment has its own set of biasing and control lines and its own analogue signal output. Such a solution increases the readout speed by parallel operation and it allows using at least part of the detector in case of defects in other areas of the chip. Since all the peripheral elements of the readout circuit as well as detector guardrings are designed only from

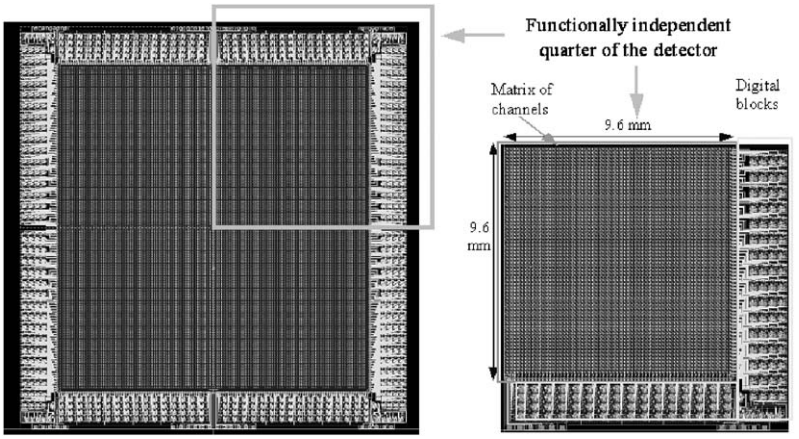

Fig. 5. Layout of the prototype of the full-scale SOI sensor with integrated digital control blocks.

the two neighbouring sides of the sub-segment, there is no dead area between detector quarters.

The sensor's I/O pins are placed at the top and the bottom side of the chip, which allows building longer detector ladders with small dead areas between chips. To improve reliability of the chip, the I/O pins are equipped with pad protection circuits in the form of two well diodes and guardrings.

The sensor active area is surrounded by a detector guardring. Such a guardring in SOI technology requires etching a trench in the upper silicon layer and the buried oxide. In order to avoid leading digital and analogue signals from the readout matrix over the trench, the guardring has a form of elongated pixels connected by a common polarization line.

Such a detector, according to simulation results, should work with readout frequency clock up to 1 MHz. It was designed to cover up to 300 MIP dynamic range with a voltage signal of 6.8 mV per MIP. In the end of 2004 the first prototype was produced and it would be soon tested.

5. Conclusions

A novel solution for the active pixel detector was proposed. The new detector as a monolithic device allows reduction of the total sensor thickness and elimination of the expensive and complicated bump-bonding process. On the other hand, the developed detector due to the electrical separation of electronics and detector active layers may give possibility to overcome the limitation of the well-established CMOS sensors.

Recently small-area SOI detectors have been produced and tests of the detectors were performed. Their functional blocs validate the concept of the novel device. Further stages of the development will concentrate on further studies of the full size detector performance.

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References

[1] A. Chediak, et al., SIMOX—the winner for 300 μm SOI wafer fabrication, Berkeley, University of California, 2002. Available at www.mse.berkeley.edu/faculty/sands/MSE125%2520alias/TICS5GRP7.pdf.
[2] M. Caccia, et al., Nucl. Phys. B 125 (2003) 133.
[3] M. Amati, et al., Nucl. Instr. and Meth. A 511 (1–2) (2003) 265.

[4] M. Baranski, et al., TSSOI as an Efficient Tool for Diagnostics of SOI Technology in the IET, Proceedings on Diagnostics & Yield 2003, Warsaw, Poland, 2003.
[5] H. Niemiec, et al., Technology development for silicon monolithic pixel sensor in SOI technology, Proceedings of the Tenth International Conference MIXDES 2003, Lodz, 2003, pp. 508–511.
[6] J.D. Berst, Monolithic Active Pixel Sensors for High Resolution Vertex Detectors, Proceedings of the Sixth Workshop on Electronics for LHC Experiments, Krakow, Poland, 2000, pp. 535–539.
[7] A. Czermak, et al., Data acquisition system for silicon ultra fast cameras for electron and gamma sources in medical applications (SUCIMA Imager), Presented at the Eighth ICATPP Conference on Astroparticle, Particle, Space Physics, Detectors and Medical Physics Applications, Como, Italy, 2003.
[8] Eastman Kodak Company, Shutter operations for CCD and CMOS image sensors, Application Notes, 2001. Available at http://www.kodak.com/global/plugins/acrobat/en/digital/ccd/applicationNotes/ShutterOperations.pdf.