Development of a prototype module for a DEPFET pixel vertex detector for a linear collider

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***Abstract*— For operation at a linear collider the excellent noise performance of DEPFET pixels allows building very thin detectors with high spatial resolution and low power consumption. However, high readout speeds of 50 MHz line rate and 20 kHz for the full detector must be reached. A prototype system is presented, using a new DEPFET pixel matrix (128 x 64 pixels), fast steering chips (Switcher II) for row wise operation and a fast current based readout chip (CURO II). The sensors with small linear DEPFET pixels (22 x 36 μm^2) are optimized for fast readout and high spatial resolution. Measurements show that the complete removal of the accumulated signal charge from the internal gate (complete clear), which is fundamental for the foreseen readout mode, is feasible. The current based readout chip CURO II, containing current memory cells, pedestal subtraction and on chip zero suppression for a triggerless operation has been fabricated and tested. First results of a full prototype system are presented.**

I. Introduction

The high energy electron-positron collider ILC (International Linear Collider) is the ideal complement to the hadron collider LHC, allowing excellent efficiency and purity in the flavor identification of hadronic jets. The separation between b and c decay tracks and the distinction between their primary, secondary and tertiary vertex should become possible. In order to minimize multiple scattering contribution to the impact parameter resolution the reduction of material of sensor and cooling in the detector area requires close attention. Consequently a thin detector with high signal to noise and low power consumption is needed.

In addition the background conditions and time structure of the accelerator influence the the design of the vertex detector. Due to very prominent beamstrahlung near the interaction point the number of hits in layer 1, typically situated at a radius of 15 mm just outside the beam pipe, for each bunch crossing and per mm^2 is 0.03 (0.05) for $\sqrt{s} = 500(800)GeV$ and a magnetic field of 4 T [6]. With a bunch structure of 2820 bunches within $950\mu s$ it becomes inevitable to keep the pixel size small and read out the detector several times during the train in order to keep the detector occupancy at a level that does not compromise the track reconstruction.

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II. DEPFET Concept for a e+e- Linear Collider

In the DEPFET Pixel concept as shown in fig. 1 the first amplifying p-channel transistor is integrated into a fully depleted high resistivity silicon substrate [1].

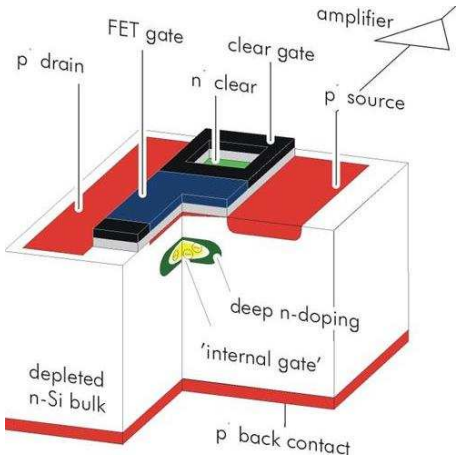

Fig. 1. *Schematic cross section of the DEPFET pixel detector.*

By sidewards depletion and an additional n-implantation below the FET, a potential minimum for electrons is created right underneath the transistor channel which can be considered as an internal gate of the FET. The signal electrons created by an impinging particle are collected and stored in the internal gate, which leads to a change in the potential of the internal gate resulting in a modulation of the transistor channel current. As the operating state of the FET has no impact on the collection of signal charge, the dead time and the power consumption can be held extremely low. Due to the non-destructive readout of the pixel device the charge in the internal gate has to be removed from time to time. This 'clearing' is obtained by periodically applying a positive voltage pulse to a separate

contact at the border of each pixel (pulsed clear mechanism). Other clear mechanisms have also been studied [4].

In this concept, stray capacitances due to connections between sensor and amplifier are vastly reduced and a very small input capacitance can be realized. This leads to a excellent noise performance. With single isolated DEPFET pixels, an equivalent noise charge of $ENC = 2.2 \pm 0.1\, e^-$ at room temperature has been measured [3]. For a large DEPFET matrix operated at a readout speed required for the ILC, a total noise figure of $ENC = 100\, e^-$ or less is aimed for. In addition to the excellent signal to noise ratio new sensor devices enable small pixel sizes in large matrices and low power consumption. These features make DEPFET pixels very attractive for future particle physics experiments, especially those at a planned linear collider. In addition to the requirements above also a very high readout speed and low material budget must be reached.

The readout concept for arrays of DEPFET pixels is illustrated in fig. 2. The gate and clear contacts of the pixels are interconnected row-wise by aluminium traces, wire bonds are used for the connection with the steering chips. The drains of the transistors are interconnected column-wise and can be contacted at the bottom and/or top of the matrix to the readout chip. The pixels are read out row-wise by applying a voltage to the external gates of the DEPFETs. As mentioned above, switching off the pixels is possible independently of the amount of charge carriers in the internal gate, in particular the sensitivity is not affected by the operating condition of the FET. At the bottom of each column the current of the active pixel is transferred to one channel of the readout chip. This allows random access to the individual pixels in the matrix.

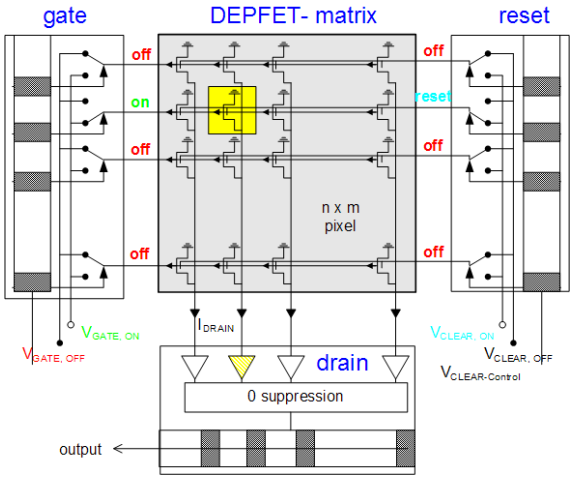

Fig. 2. *Principle of operation of a DEPFET pixel matrix.*

The expected occupancy at the innermost layer of the ILC vertex detector requires a readout rate of 20 kHz [6]. For an envisaged matrix size of 400×5000 pixels this leads to line rates of 50 MHz with the matrix being read out from both sides.

The total power consumption has been calculated using measured currents and voltages of the chips and matrices described below and assuming that they can be switched off during between subsequent bunch trains, as a duty cycle of 1/200 is foreseen at the ILC. Scaled to the total pixel vertex detector [6] primarily designed for TESLA with 5 layers, the sensor is expected to have a power consumption of 0.3W, while the ICs consume $\sim 3-4$W (steering) and $\sim 1-2$W (readout), respectively. Hence, we consider a total power budget of less than 5W for the entire vertex detector is feasible.

III. The Prototype System

In the development to this goal a USB-based prototype system, including a new DEPFET matrix with small pixels and dedicated ASIC chips for fast steering and current based readout, has been developed. The main components of the system are shown in fig. 3.

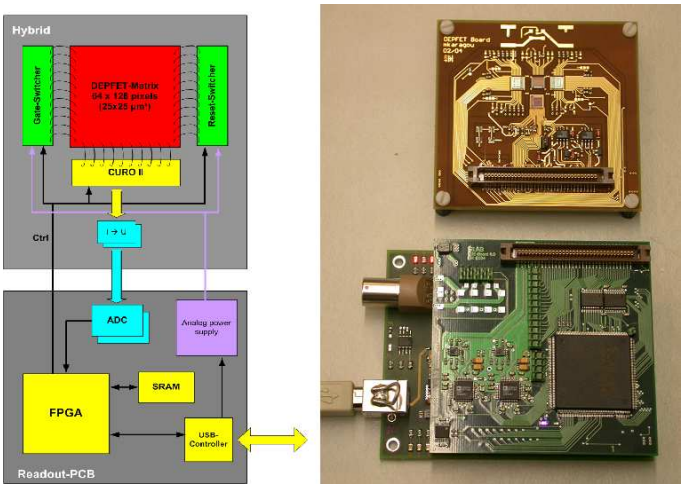

Fig. 3. *Block diagram and photo of the readout and hybrid pcbs.*

For greater flexibility with regard to laser or testbeam setups it is subdivided into two parts, connected by a ribbon cable. The sensor matrix as well as the ASICs for steering (Switcher II) and readout (CURO II) are assembled on one hybrid PCB, while the digitally parts like FPGA, USB controller, ADCs and RAM are assembled on a separate PCB. Besides those pcbs merely external power supplies and a PC are needed for operation. In the following the main components of the system will be discussed.

A. Switcher II

The selection of a particular row as well as the Clear are controlled by the 2x64 channel SWITCHER II chips, which are developed in Bonn in 2002 and fabricated with an AMS 0.8 μm high-voltage process. The chip is capable of switching voltages up to 20 V with frequencies of >30 MHz. A RAM on the chip stores the control sequence allowing operation modes with no external control signals. Several chips can be daisy chained if more than 64 channels are to be addressed. For a detailed description of the Switcher chip see [8].

B. CURO II

The 128 channel CUrrent Readout Chip (CURO II) was developed in Bonn and fabricated at TSMC in a 0.25 μm CMOS technology with a radiation tolerant design. The readout architecture is based on a current mode signal processing scheme, well adapted to the output of the DEPFET pixels, which are currents, not voltages. The principle of the readout is shown in fig. 4.

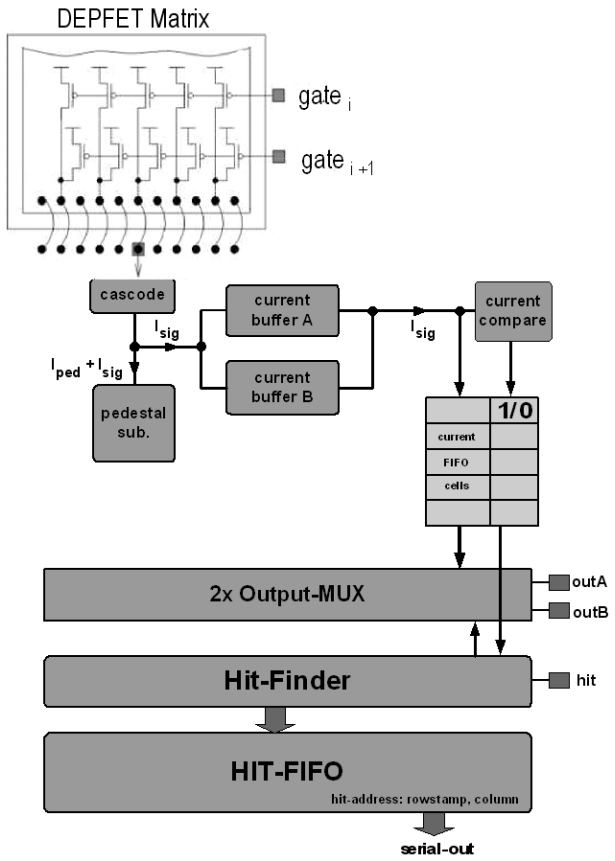

Fig. 4. *Readout principle of CURO II.*

The functionality of the readout chip can be separated into two major parts.

In the first part, a regulated cascode keeps the pixel drain at a constant potential, eliminating the influence of the large sensor capacitance and the effect of the limited output conductance of the pixel transistor itself. After selecting one row of the matrix, the current is stored in a fast current memory cell. By applying a positive voltage pulse to the Clear contacts of the same row the accumulated signal charge is removed from the internal gate. The so derived pedestal current is subtracted from the buffered current automatically at the output node of the memory cell due to its inverting character. The resulting signal current is stored in a further memory cell.

In the second part of the readout chip, a digital hit pattern is determined by comparing the buffered currents of a row with individual thresholds in parallel. Since only those memory cells with values above the threshold are needed, all other cells are switched off in order to save power. A digital hit finder identifies up to 2 hits in the digital pattern of a row per cycle and processes a row until no more hits are found. The pixel address, i.e. row and column, of an identified hit is stored in a digital hit buffer, while the corresponding analog value is multiplexed to one of the two output channels immediately. A more detailed description is given in [2].

C. Readout Board

The output current of CURO is converted into a differential voltage signal by an external low noise and fast transimpedance amplifier, then digitized by a 14 bit ADC and stored in SRAM cells for a subsequent readout. The slow control and readout of the chips, the sophisticated timing, the fast storage of ADC values in the RAM and the data transfer to the PC via USB is managed by a SPARTAN 3 FPGA. Furthermore, a software-programmable Sequencer inside the FPGA is used to control and optimize readout modes easily. The main system clock is digitally adjustable in a wide range. In order to minimize crosstalk all clock signals are distributed as LVDS signals.

D. CMOS Test Matrix

In order to show the functionality of the readout system independently from the properties of a new DEPFET matrix, a dedicated CMOS Test Matrix has been developed [7] and fabricated in CMOS 0.35 μm technology. Since the CMOS 3.3V technology is well understood, such a test matrix is much easier to integrate in a new system than a DEPFET matrix and is thus very valuable for debugging purposes. The Test Matrix has 64×128 cells with an identical pad layout as the DEPFET counterpart. Every pixel cell contains an NWELL-PSUB photodiode and a circuitry that generates an offset current and an illumination dependent current, analog to an increase of DEPFET current caused by an impinging particle.

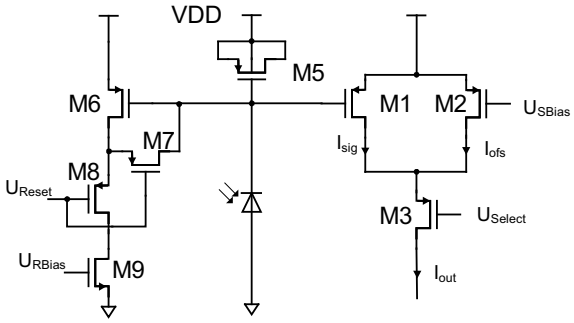

Fig. 5. *Circuit of a Test Matrix pixel cell.*

The circuit of a pixel cell is shown in fig. 5. The offset current of $\sim 30 \mu A$ is generated by a constant current source M2, whereas the voltage controlled signal current source is regulated by the voltage across capacitor M5. Capacitor M5 is charged by the photo current generated in the photo diode. By closing the Select switch M3 the sum of signal and offset current is applied to the output of the pixel cell. The reset mechanism is designed in a way, that the capacitor M5 is not

discharged to zero, but to the threshold voltage of transistor M1. Thus, the illumination of a pixel cell after a reset leads to an increase of the output current instantaneously. The normal way of discharging M5 to the threshold voltage of M1 would be using a very small reference current of the current mirror given by M9. But that slows down the reset procedure. Therefore, a larger reference current of $\sim 10\mu A$ is used but the W/L of transistor M6 is chosen 30 times larger than the W/L of transistor M1. Thus, the signal current after a reset is in the regime of nano amperes and is therefore negligible compared to the offset current. The time required for the reset has been measured to $< 6ns$ [7].

Fig. 6 shows a picture taken with the prototype system, using a simple webcam lens mounted on the hybrid equipped with a CMOS Test Matrix. The readout of the 128 x 64 pixels was done within $\sim 1ms$, which is equivalent to $\sim 120ns$ per pixel.

Fig. 6. *Picture taken with full prototype system equipped with CMOS Test Matrix and webcam lens. (from left to right: R. Kohrs, C. Sandow, M. Trimpl and H. Krüger.)*

E. DEPFET Matrix

The DEPFET matrices are processed in a MOS technology with two polysilicon and two metal layers on high ohmic n- substrate, developed and fabricated in 2004 at the semiconductor laboratory of the Max-Planck-Institutes in Munich [5]. Along with the R&D for HEP vertexing, the DEPFET technology was changed from JFETs to MOSFETs as MOSFETs have a number of advantages, e.g. allowing much smaller pixel sizes, providing a better homogeneity and a potentially higher internal amplification. A very compact linear pixel cell geometry has been introduced, where the implanted drain, source and clear regions are shared by neighboring cells (double pixels). Furthermore, a polysilicon structure, the so called 'clear gate', supports the clear process, and acts as an isolation frame between clear region and internal gate during the charge collection. A variety of slightly different structures were processed in order to determine the optimal parameters by means of the fabrication process, pixel size, charge collection efficiency and clear efficiency. The smallest pixel size so far is $22 \times 36\mu m^2$. Simulations have confirmed that no potential pockets, which can trap signal charges during charge collection and clearing, exist in the design. A more detailed description is given in [5].

The figure of merit of the DEPFET is the transconductance of the internal gate $g_q = dI_D/dQ$, where dI_D is the change of the drain current and dQ is the collected charge in the internal gate. A value of $g_Q = 0.4nA/e^-$ has been measured in very good agreement with the simulations.

Equivalent Noise Charges of $ENC = 9.8e^-(\sigma)$ have been measured with a linear double pixel structure at room temperature (fig. 7).

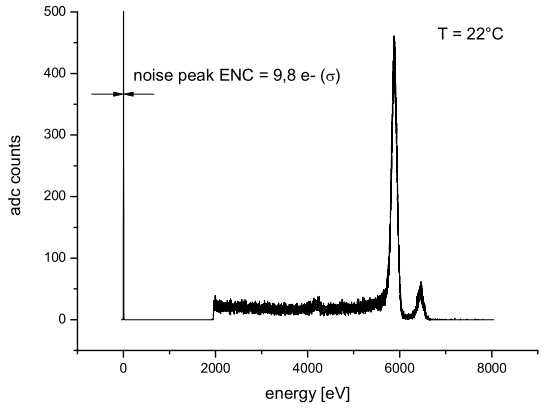

Fig. 7. *^{55}Fe Spectrum taken with a linear DEPFET structure at room temperature.*

One contribution to the overall noise of the signal is the incomplete removal of charges of the internal gate, as the pedestal subtraction in CURO is done 'on the fly' (see fig. 8).

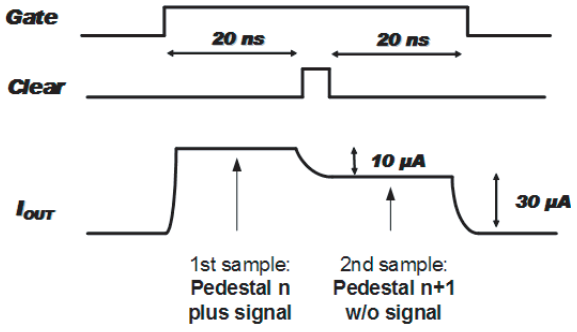

Fig. 8. *Readout sequence of a DEPFET with 'on the fly' pedestal subtraction.*

The difference of the two current samples taken by CURO is thus not just the pure signal value but also the uncertainty of charge left in the internal gate after an incomplete clear. Therefore a complete clear is essential. Measurements on double pixels and small matrices show that a complete clear is feasible with moderate voltages of ~ 14V, which is easily achievable with the Switcher chip.

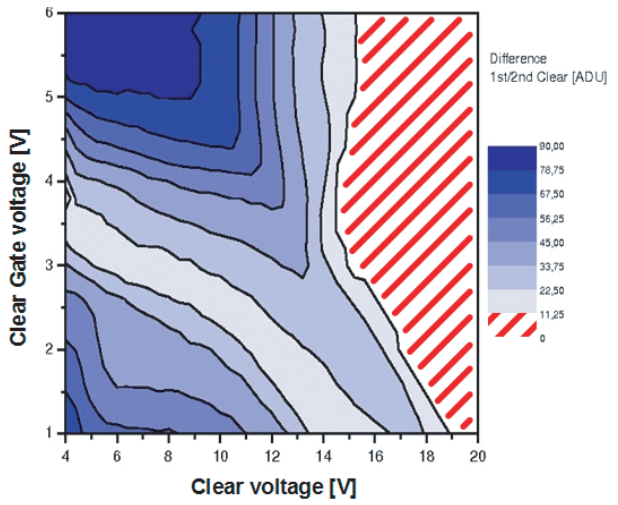

Fig. 9. *Difference between two current samples. The hatched area indicates an efficient Clear.*

Shown in fig. 9 is the difference of two current samples, with a charge injection by laser and a subsequent clear pulse in between. In the case of a residual current of zero the charge in the internal gate is the same before and after the clear, but not necessarily zero. The proof of a *complete* clear is shown in fig. 10, where the width of the noise peak obtained by measuring the DC DEPFET drain current is plotted, using two different readout operations: (a) a single Clear pulse followed by 500 samples, (b) 500 individual Clear pulses, immediately followed by a readout sample. If the charge removal is complete the clear noise contribution vanishes and the noise level drops, thus, the widths of the noise peaks in both cases should be the same.

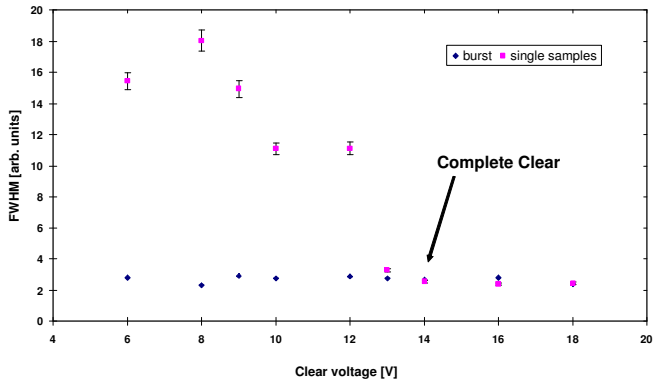

Fig. 10. *Evidence for a complete Clearing of the internal Gate for voltages larger than 14 V.*

IV. Conclusion

A full prototype system including a new DEPFET matrix and dedicated ASIC chips for steering and readout have been developed addressing the demanding requirements of the ILC.

Performance measurements on the main components of the system can be summarized:

- The steering chip Switcher 2 is versatile and works fine up to $> 30MHz$ providing voltage levels sufficiently for a complete Clear.
- All measurements done on the readout chip CURO with its fast current memory cells, correlated double sampling, on-chip pedestal subtraction and triggerless zero suppression are in agreement with the simulated performance.
- The new DEPFET matrices with small pixel sizes show low noise, complete clear and an improved internal gain.

The functional efficiency of the prototype system was adduced with a dedicated CMOS Test matrix. It is now ready for operation with the new DEPFET matrices, which have already been tested separately. The full system will be characterized in a testbeam in the beginning of 2005.

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