A DEPFET pixel matrix system for the ILC vertex detector

M. Trimpl[a] *, L. Andricek[b], P. Fischer[c], R. Kohrs[a], H. Krüger[a], G. Lutz[b], H.G. Moser[b], I. Peric[c], M. Porro[d], L. Reuen[a], R.H. Richter[b], C. Sandow[a], L. Strüder[d], J. Treis[d], N. Wermes[a]

[a]Physikalisches Institut der Universität Bonn, Nußallee 12, D-53115 Bonn, Germany

[b]Max-Planck-Institut für Physik, Föhringer Ring 6, D-80805 München, Germany

[c]Institut für Technische Informatik, B 6, 26, D-68131 Mannheim, Germany

[d]Max-Planck-Institut für extraterrestrische Physik, Gießenbachstrasse, D-85740 Garching, Germany

The DEPFET detector offers radiation detection and amplification jointly by embedding a field effect transistor into fully depleted silicon. Due to the excellent noise performance (ENC = 2.2 e^- for single pixel at room temperature) and the high spatial resolution (4.3 μm at 22 keV with 50 μm^2 pixels) of the device, DEPFET pixels are attractive for XRAY astronomy, for biomedical application and for tracking in particle physics. For the vertex detector of a future TeV-scale linear collider, like the proposed ILC (International Linear Collider), a highly granulated pixel system operated row-wise with line rates up to 50 MHz is needed. Addressing these requirements, improved DEPFET sensors with 22x36 μm^2 pixels and dedicated chips for steering and readout have been fabricated and operated in a current based mode offering a thousand times faster readout than achieved so far. Moreover, the results presented in this paper give a detailed characterization of the entire system concerning readout speed, accuracy and noise.

Keywords: readout electronics, Switched Current, Linear Collider, ILC, Active Pixel Sensor, DEPFET, CURO

1. Introduction

A TeV-scale linear collider, like the ILC, offers a large variety of precision measurements complementary to the discovery potential of the large hadron collider (LHC). To fully exploit this physics potential a vertex detector of unprecedented performance is needed providing a pure and efficient b and c tagging. For the first time, the detection of the vertex charge will allow the discrimination between b and $\overline{\mathrm{b}}$, and between c and $\overline{\mathrm{c}}$ jets. While state of the art pixel systems like hybrid pixels or conventional CCDs can fulfill the requirements of present experiments, new pixel developments are necessary for future linear colliders, where thin detectors with less than 0.1 %X_0 material per layer, an extremely low power consumption and small pixel sizes of 20-30 μm square are needed [1].

*Corresponding author Marcel Trimpl, Tel.: +49-228-73-2499; fax: +49-228-73-3220. E-mail address: trimpl@physik.uni-bonn.de

Since the accelerating system of the ILC has been decided to be a superconducting one, the timing structure of the bunch train is fixed. Due to the prominent e^+e^-- beamstrahlung near the interaction point (80 hits / mm^2 / bunch train at r=15 mm) a multiple readout (10-30 times) of the vertex detector during the bunch train is inevitable to keep the occupancy at a reasonable level. Reading out the whole vertex detector containing almost 10^9 pixel in 40 μs, line rates of several ten MHz in the ladders are required. At the same time, a noise figure of around 100 e^- is favored. Facing these challenging requirements, the DEPFET detector is a promising approach for a future micro vertex detector.

2. The DEPFET concept for a micro vertex detector

DEPFET sensors offer a first amplification stage in the form of a field effect transistor inside the sensor pixel [2]. The high resistivity sen-

sor material is fully depleted by means of sidewards depletion, forming a potential minimum for electrons underneath the transistor channel, the internal gate. Electrons created by impinging particles are accumulated in the internal gate, insensitive to outer electro-magnetic disturbances and modulate the transistor current. Thus, the device offers intrinsically a complete charge collection. In this context the figure of merit of the DEPFET is the amplification of the internal gate, $g_q = dI/dQ$, where dI is the change of the device current and dQ is the accumulated charge in the internal gate. Values of up to $0.4\,\mathrm{nA/e^-}$ have been measured with present devices [3] in perfect agreement with simulations, more aggressive pixel designs propose a gain of up to $\mathrm{g_q} = 1\,\mathrm{nA/e^-}$ [4]. As the charge remains in the internal gate by probing the transistor current, DEPFET pixels need an external reset mechanism, also called the clear of the internal gate. The reliability of the clear mechanism has already been proven [5] as it is essential for providing a stable pedestal reference in an ILC operation mode.

Pixels in a matrix are addressed like in a RAM structure: One row is selected after each other and the pixel currents are probed column wise at the bottom of a matrix. Such a row-wise operation mode features a very low power consumption being a crucial criteria of the cooling scheme at a future linear collider. Due to the internal amplification and due to the possibility of making small pixels the particular attributes of the DEPFETs are an excellent noise performance and a high spatial resolution at the same time [6]. For a micro vertex detector the low noise can be exploited in terms of building thin devices in the order of $50\,\mu\mathrm{m}$ [7] still offering a reasonable signal to noise ratio of about 50.

3. The ILC DEPFET-System

A photograph of the ILC DEPFET-System is shown in figure 1. It consists of two major parts, a sensor PCB (left) and a stack of DAQ-boards (right), both connected by a ribbon cable to maintain higher flexibility. The DAQ-boards provide an USB based communication with a PC, configure the steering and readout chips and digitize and store the analog data. The sensor PCB hosts the DEPFET pixel matrix driven by two steering chips SWITCHER II for row selection and reset. The columns of the matrix are read out in parallel at the bottom by the CURO II chip (see figure 2).

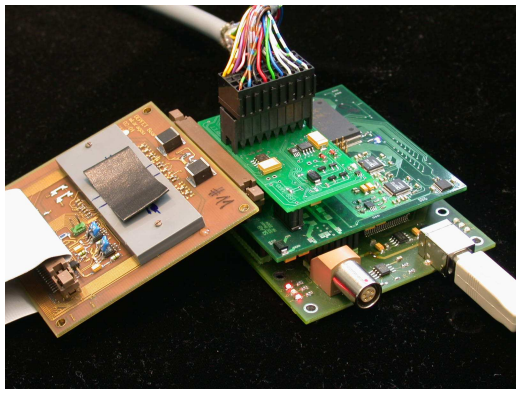

Figure 1. Photograph of the ILC DEPFET-System. The sensor matrix and the chip assembly are protected by a plastic cap on the sensor PCB.

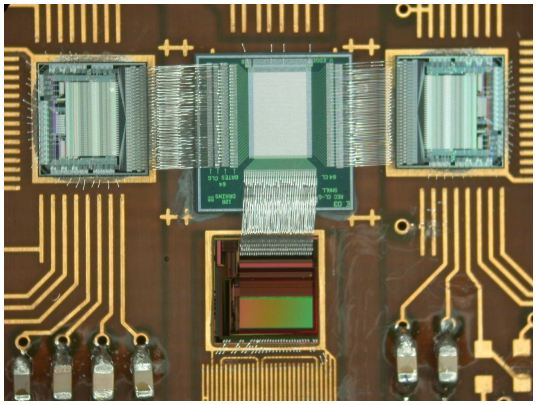

Figure 2. Micro photograph (area shown: $23\mathrm{x}16\,\mathrm{mm}^2$) of the chip arrangement on the sensor PCB, a 64x128 pixel DEPFET-Matrix (middle), two steering chips SWITCHER II (left & right) and the readout chip CURO II (bottom).

Since a fast readout is one of the crucial points of the ILC-system a completely current based approach has been chosen, the CURO (**CU**rrent **R**ead**O**ut) Architecture. It is well suited to the signal of the DEPFET, which is intrinsically a

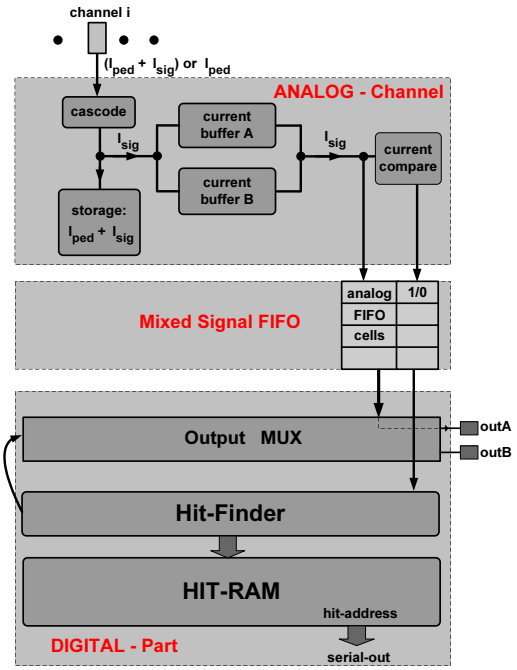

Figure 3. Readout principle of the CURO-Architecture.

current. Upon the many advantages of the current mode signal treatment, the most important ones are: A high dynamic range can be preserved while supply voltages decrease in modern chip technologies, and, a very convenient and accurate subtraction of two currents is possible, like it is needed for a pedestal subtraction. The readout principle of the CURO-Architecture is illustrated in figure 3. The input stage is realized by a regulated cascode providing a low input impedance for the DEPFET current. In this context, the readout speed is no longer limited by the transimpedance of the DEPFET pixel, which is preferably kept low to obtain good noise figures. In addition, the performance of the cascode circuit can be tuned in terms of power according to the capacitive load at the drain node. After one row in the sensor matrix has been selected for readout, the signal current of the pixel superimposed by a pedestal current $I_{sig} + I_{ped}$ is stored in a current memory cell. A detailed description of the current memory cell can be found in [8]. The row is then reset and the remaining pedestal current provided by the sensor I_{ped} is automatically subtracted at the memory cell. The resulting signal current I_{sig} is stored alternately in two buffer cells. In the subsequent cycles the front end is ready again for a new DEPFET row. Meanwhile, the signal current in the buffer cell is compared with a programmable threshold and the digital result is stored together with the analog value in a small mixed signal FIFO. Simulations show that a FIFO depth of 4 rows is enough for the occupancy expected at the ILC. The currents in the FIFO below the threshold are not relevant any more and the digital pattern can be used to switch off the appropriate analog FIFO cells to save power. One can think of a more sophisticated cluster logic, keeping the neighbors of a seed pixel, as well. The realization of such a logic will strongly depend on the observed cluster size in a test beam experiment. Note, that the whole front end is operated by one single LVDS clock, synchronous to the row clock of the matrix. All control signals for the complex analog part are derived from this clock inside the chip. To empty the FIFO, a fast parallel arranged hit finder, as proposed in [9], analyzes the digital hit pattern and finds up to 2 hits per cycle. Their addresses are stored in a Hit-RAM and the analog values are multiplexed to 2 output nodes where they are digitized by two external ADCs on the DAQ-boards. When the Hit-RAM is full, it is read out by the DAQ-boards and the hit addresses are merged with the analog values.

4. Performance of the ILC-System

4.1. Matrix steering - SWITCHER II

The SWITCHER II chip's purpose is to steer the DEPFET matrix in terms of row selection and clearing. To cope with the high voltage ranges needed for the proper clearing operation it has been fabricated using an AMS 0.8 μm high voltage process. The digital part of the switcher chip, e.g. mainly the RAM storing the steering sequences for a DEPFET row, works up to 80 MHz. The analog switching performance is given by the resistance of the output stage and the capacitive load that is driven. Measurements on the output resistance of SWICTHER II (see figure 4) show values in the order of 200 Ω for the NMOS

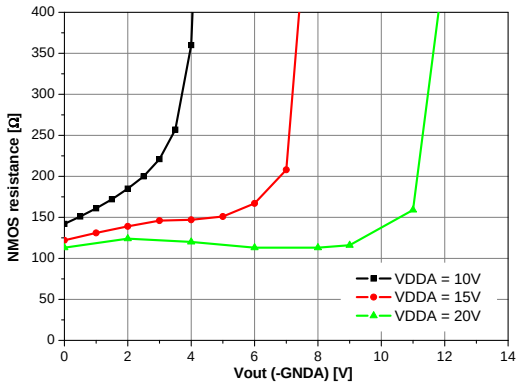

Figure 4. Output resistance (NMOS part) of SWITCHER II versus the output voltage for three different analog supply voltages.

part depending on the supply and steering voltage. Similar values of well below 500 Ω have been observed for the PMOS part of the output stage. Driving a DEPFET-row with a typical load of 15 pF would therefore yield a rise time of $\tau \leq 3$ ns.

4.2. Current based readout - CURO II

Based on the results of the prototype chip CURO I [8] a 128 channel readout chip has been fabricated in a TSMC 0.25 μm, 5 metal process. In this first version of CURO II only one analog FIFO row has been implemented, so that the readout has to be interrupted if more than two hits are found in a row. For a continuous analog readout coping with higher occupancies the analog FIFO size can be scaled easily to a suitable size in a future chip version. Furthermore, a continuous binary operation with high occupancies is possible, as the full digital FIFO size is implemented.

The digital part of the chip, e.g. hit detection and zero suppression, works up to 110 MHz, outperforming the expected hit occupancy at the ILC by a factor of 2.

The linearity of the complete analog part, e.g. the input cascode and 3 successive sampling stages (pedestal subtraction, buffer and FIFO cell), is shown in figure 5. All measurements concerning the analog part are performed with a double sampling rate of 24 MHz. That means that two samples (pedestal and signal) are performed

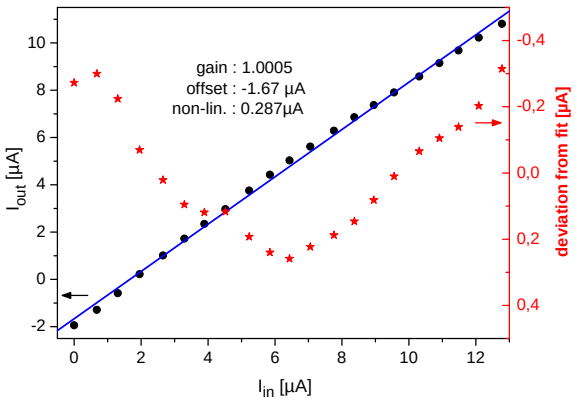

Figure 5. Linearity of the total analog part of CURO II at 24 MHz double sampling rate (The points indicate the output current, the stars indicate the integral non-linearity).

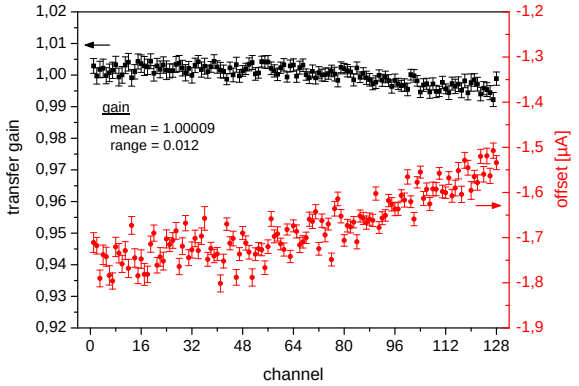

Figure 6. Homogeneity of the transfer gain (squares) and offset (points) of the analog part of CURO II.

within roughly 40 ns. The capacitive load at the input node was approximately 10 pF. Although the bandwidth of the chip has been designed to be higher than 50 MHz, the maximum analog frequency is fixed to 24 MHz by the present readout system. The analog part has a transfer characteristic close to 1 and an integral non-linearity of 2.3 % for a dynamic range of 12.5 μA, equivalent to several mips. Gain and offset for all 128 channels are shown in figure 6 . Due to the properties of the memory cell is the transfer behavior in first order insensitive to fluctuations of the supply voltage and a narrow dispersion of the gain with a total range of 0.012 is achieved. Any in-

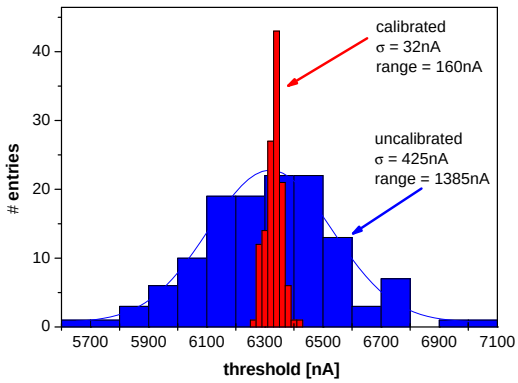

Figure 7. Dispersion of the comparator threshold (128 channels) before the internal calibration and after two calibration cycles.

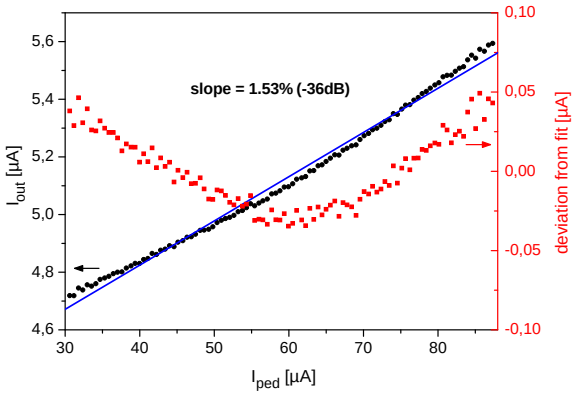

Figure 8. Performance of the pedestal subtraction in the front-end of CURO II at 24 MHz double sampling rate for $I_{sig} = 6.8\,\mu$A.

homogeneity of the offset is of minor importance since it can be compensated by a threshold calibration using a 5 bit DAC in every column (not shown in figure 3), so that a global threshold can be used for the current compare. After two calibration cycles the remaining threshold dispersion for all 128 comparators is σ=32 nA (see figure 7), which is already below the expected noise figure of the analog part. Once the comparator unit has been calibrated to one global threshold, the calibration data can be used for different thresholds without a noticeable widening of the dispersion. The quality of the pedestal subtraction is given in figure 8 where the output current is plotted versus the pedestal current for a constant signal current. The linear dependency complies with a pedestal suppression of -36 dB. Assigning this performance to a DEPFET matrix with a statistical spread of 5 μA in the pedestals, a variation of 75 nA would remain after pedestal subtraction. Furthermore, the pedestal subtraction is uniform for the whole chip, as a mean slope of 1.50 % and a total dispersion of 0.26 % for all 128 channels has been observed.

4.3. Power consumption

The power consumption of the present SWITCHER and CURO chips has been measured at the target row rate of 50 MHz. The CURO requires 2.8 mW per channel, out of which approximately 400 μW are used in the cascode input stage. The SWITCHER dissipates 6.3 mW per channel at 50 MHz, whereas 0.5 mW per channel is needed as static power for the idle steering chips in the detector ladder to ensure that their pixels are turned off. The reduction of the DC power consumption as well as a fast power-on/off feature is one of the main design goals for the next chip generations. The contribution of the DEPFET sensor to the total power is small as merely a few rows in the large ladders are selected at the same time and a single pixel consumes not more than 500 μW. Scaled to a full vertex detector [1] a total power consumption of 4 W is expected (0.5 W sensor, 2 W steering and 1.5 W readout) operated in a duty cycle perfectly synchronized to the bunch train. This figure can be handled by a simple cooling gas without adding further solid material into the active detection volume.

4.4. Operation of a 64x128 ILC DEPFET-Matrix

The complete system has been tested using a 64x128 pixel ILC DEPFET-Matrix (450 μm sensor thickness with 22x36 μm^2 pixels). A 3.3x2.6 mm^2 and 10 μm thick tungsten absorber foil with an engraved logo has been placed onto the sensor and irradiated with a ^{55}Fe radioactive source. Taking the radiogram shown in figure 9 the readout cycle for one matrix row was approximately 1.5 μs long. Although the single components of the system have been approved to much higher rates, the system speed has been chosen

Figure 9. Radiogram of a 10 μm thick tungsten logo irradiated by ^{55}Fe taken with the ILC-DEPFET system.

that slow to ensure a stable operation of the entire system without optimizing the critical timing of the components. The overall system noise performance achieved was ENC $< 250\,e^-$.

5. Conclusion

An ILC DEPFET-system equipped with a 64x128 pixel matrix has been developed and operated successfully with two dedicated chips for steering and readout.

The steering chip SWITCHER II can drive capacitive loads faster than 0.5 ns/pF for high voltage ranges up to 25 V, sufficiently high to guarantee a proper and reset-noise-free operation of a DEPFET matrix.

The readout chip CURO II features a current based operation mode of a DEPFET matrix entering line rates in the multi-MHz-regime, more than a factor of thousand faster than DEPFET readout systems established so far. Pedestal subtraction and a fast correlated-double-sampling is done in the analog part of the readout chip with a transfer gain of 1.0005 and an integral nonlinearity of around 2 %, measured at a double sampling frequency of 24 MHz for a wide dynamic range. Facing the enormous pixel number and the harsh readout rates at a TeV-scale linear collider, stand alone hit finding and zero suppression is done inside the readout chip as well and has been successfully tested up to 110 MHz, more than a factor of 2 faster than needed at the ILC.

The complete system has been used for the spatial detection of 6 keV photons from a ^{55}Fe source, where a total noise performance of ENC $< 250\,e^-$ was achieved.

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