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Interposer development for 3D trackers

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ABSTRACT: Tracking detectors with intrinsic momentum discrimation capabilities will necessarily require communication between nearby layers to correlate hits and establish an approximate curvature determination. Interlayer communication may be approached in many ways. Herein we describe design and fabrication issues associated with a fully 3D approach in which vias through a bulk interposer provide one-to-one contact between pixels of the two layers.

KEYWORDS: Particle tracking detectors; Trigger detetectors

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1 Introduction

The present Level-1 trigger in CMS is derived from calorimeter and muon system information without the benefit of any generic tracking component. While this is expected to be adequate for the foreseen luminosities of the LHC, proposed LHC luminosity upgrades would yield high occupancy events that saturate such a trigger. [1] Simulations indicate that in this situation the trigger will incorrectly fire on low p_T events at an unacceptably high rate. Additional information is needed in the trigger system to discriminate effectively between low p_T junk events and high p_T events of physics interest.

The simulations further indicate that the addition of fine-grained tracking information can alleviate the problem in principle. [2] In practice, however, moving fine-grained information from the detector to the trigger system at high rate implies high bandwidth transmission with correspondingly high power levels and consequent increases in the material of the tracker itself. Out of this dilemma the concept of intelligent trackers has emerged, with the goal being to bring the identification of high-p_T tracks into the tracker itself and restrict the transmission of trigger information to just those objects which exceed some fixed p_T threshold. It should be noted that in this context high p_T may be as low as a few GeV.

Local track curvature determination requires two $r\phi$ measurements at different r, with the average beamspot providing the needed third point. On the back of an envelope one may easily show that for reasonable values of layer radii and hit resolution, this three-point estimate of curvature provides useful p_T resolution for tracks with $p_T < 10\,\text{GeV}$. [3] Detailed simulations reveal a threshold curve that turns on in the few-GeV range, with specific performance depending quantitatively on the geometry assumed. [4]

In this contribution we focus on a low-level technical problem that arises in considering detectors suitable for local p_T determination. We will discuss the design and fabrication of a suitable interposer intended to both hold sensors in a paired configuration with small radial separation, and also transmit signals between them so correlated hits may be identified and translated into p_T measurements. The interposer concept and the design discussed here is based on the larger picture of sensor modules using 3D integration which has been described elsewhere in these proceedings. [5]

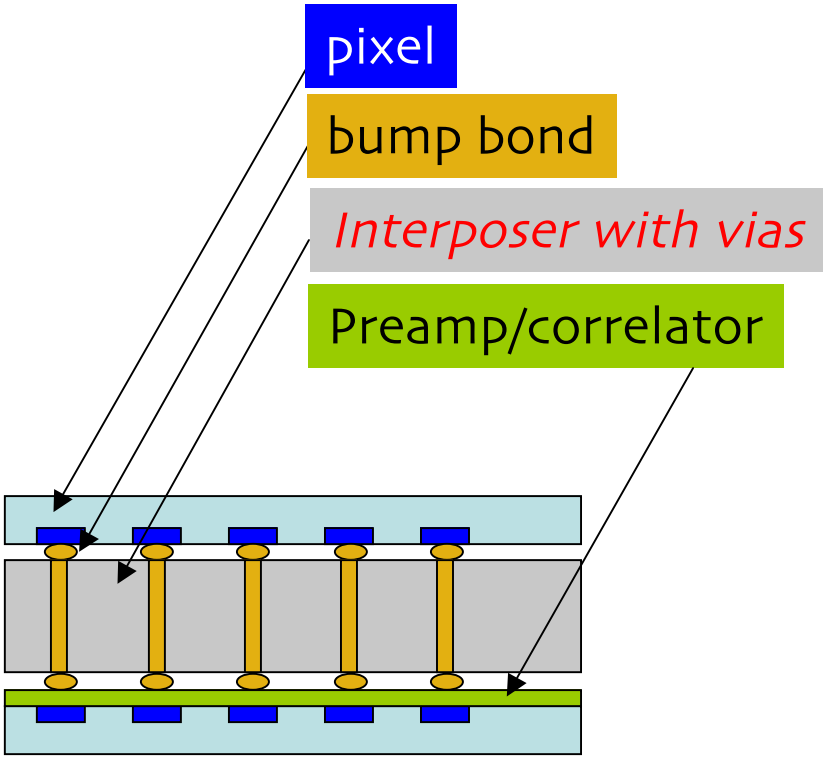

Figure 1. Schematic diagram of p_T module consisting of two pixel sensors coupled by an interposer. Each via is a conductive channel that brings the analog signal from the upper sensor to the readout and processing electronics located on top of the lower sensor. The vertical axis in this picture corresponds to the radial coordinate in the detector, and the horizontal axis to the $r\phi$ coordinate.

2 Design issues

Figure 1 shows the schematic picture of two pixel sensors with a small ($1 \sim 2$ mm) radial separation. Raw signals generated in pixels in the upper sensor are transported to the lower electronics layer by means of conductive vias in the interposer as shown.

We have fabricated prototype interposers in silicon. Although the eventual design will require an interposer of thickness 1 mm or larger, we have begun with 500 μm wafers to establish basics of the process. We etch an 8×8 array of vias, each of 150 μm diameter and set on a 600 μm pitch. These are relatively relaxed parameters, and we note that an interposer suitable for use in a real detector would require a via pitch closer to 100 μm, at least in one dimension, and consequently smaller via diameter; and as noted, greater interposer thickness. In general we observe that there are a number of issues that must be considered for a workable interposer; some of these include: (a) achievable via density; (b) achievable via diameter/length; (c) resulting electrical characteristics, i.e., the resistance and capacitance per via; (d) the manageable thickness of the interposer, which may be limited by both the via etching technology and the sputtering process used to metallize the via surface; (e) the total radiation thickness of the interposer, which should be kept to a

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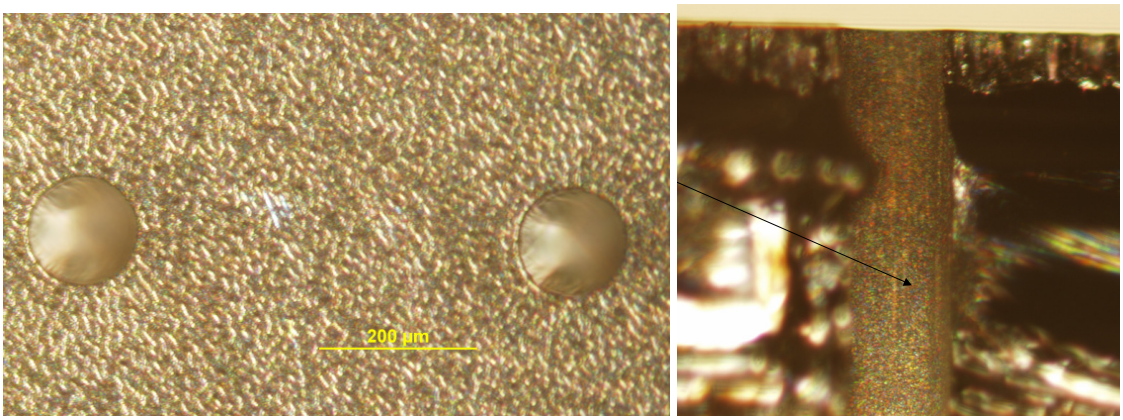

Figure 2. Left: top view of two vias after metallization (surface metalization is later removed). Right: vertical cross section of via after metallization, showing the full metal coverage of the via walls. The arrow points to the via wall.

level that is small compared to sensor thickness to limit harm to tracking and photon detection in CMS; (f) the yield and industrial feasibility of the fabrication process. Materials other than silicon, and consequently other fabrication processes will be explored in the near future. Thickness beyond ~ 1 mm may be best achieved by wafer-bonding interposers of lesser thickness. Total mass can be minimized by etching away unneeded bulk, but only insofar as mechanical strength is not unduly rcompromised.

3 Fabrication

Vias are etched using deep reactive ion etching (DRIE) technology. The via pattern is established by first growing a $1.5\,\mu$m oxide layer and then using a plasma etch to define the via location, shape, and size. DRIE then etches through the wafer; with the etcher available to us [6] the process takes 2 hours and produces a nearly vertical via wall whose taper is 1:30. Once the DRIE is complete, all oxide is removed, and then the wafer is reoxidized to ensure that the inside walls of the vias will be insulating. Metallization (aluminum or copper in the trials done so far) is then deposited on the via walls by sputtering, first from one side then from the other. Figure 2 shows the top surface and an exposed via surface after metallization.

After sputtering, the upper and lower wafer surfaces are cleaned of metal by Chemical-Mechanical Polishing. Pads for bump bonding are then laid down and the wafer is diced. At the present time the prototypes are being bonded and will be tested for electrical characteristics.

4 Conclusion

We have demonstrated that standard MEMS technology can be used to fabricate interposers in silicon. At this stage of the development the chosen geometric parameters (via diameter, spacing, and length) are modest, and future work will involve pressing towards smaller pitch, smaller diameter, and thicker interposers. Mass removal is also being currently addressed with new prototypes that were not complete at the time of this workshop.

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