Cornell University
Floyd R. Newman Laboratory for
Elementary-Particle Physics

Sensor R&D at Cornell, SiD

Argonne SiD Workshop, 6/4/2010

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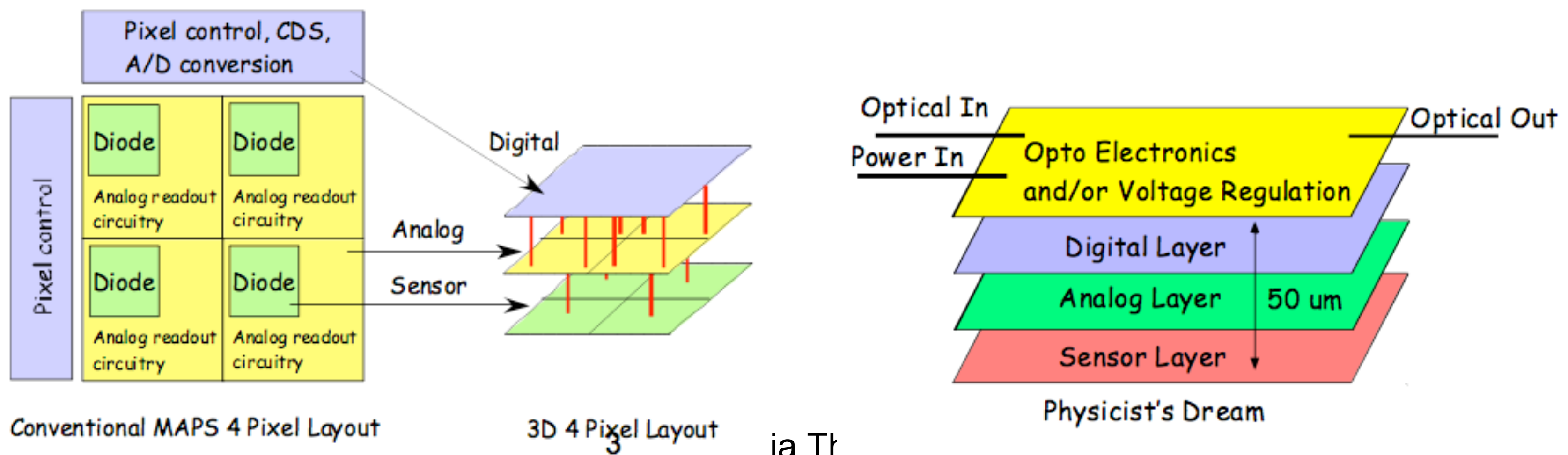
Investigating new techniques for novel HEP pixel detectors

- Trend towards miniaturization and complex circuits on thin sensors
  - monolithic detectors (e.g.MAPS), 3D integrated circuits, …
- Applications of 3D technology to future HEP detectors: S-LHC, ILC
  - Emerging “vertically integrated” (3D) devices with SOI technology
  - Attractive due to low power, high resolution, high S/N, short integration time, low material budget, radiation hardness, “edgeless” design,..
  - Ongoing R&D program at FNAL to define options for ILC application

3D concept

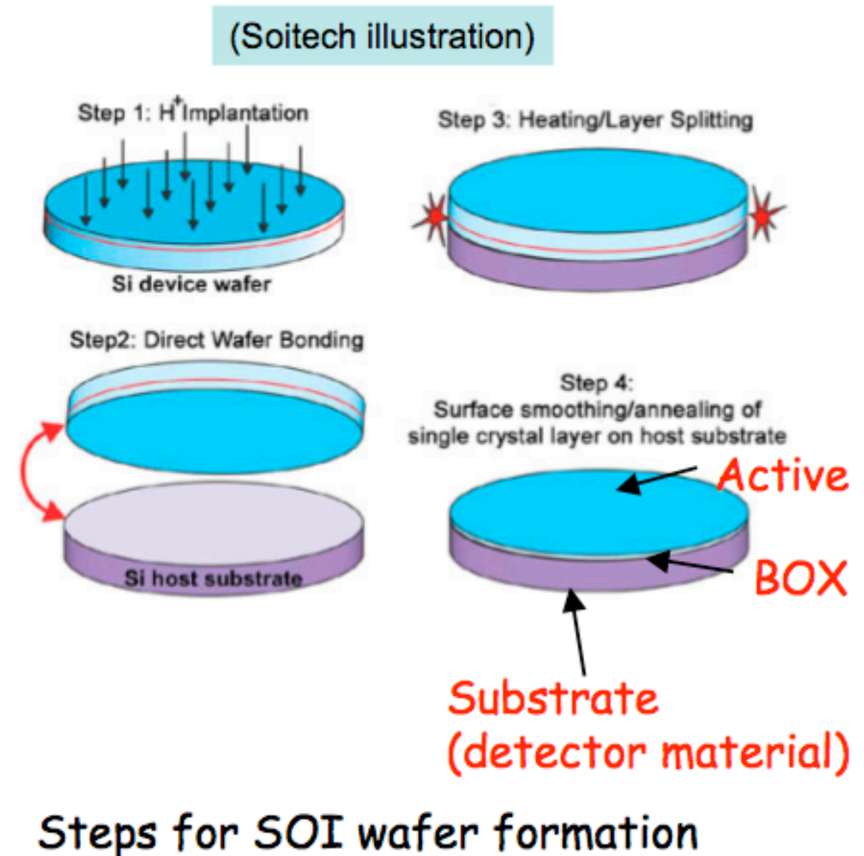
- 3D chip consists of 2 or more layers of active devices
  - Thinned, bonded, interconnected to form “monolithic” circuit
  - Layers (or tiers) can be fabricated in different processes
  - Fully active sensor area, 4-side abuttable, local data processing
  - Industry moving to 3D to improve circuit performance (reduce power, cross talk, reduce R/L/C for higher speed..)
  - Utilizes technology developed for SOI devices

From Ron Lipton:



Silicon on Insulator

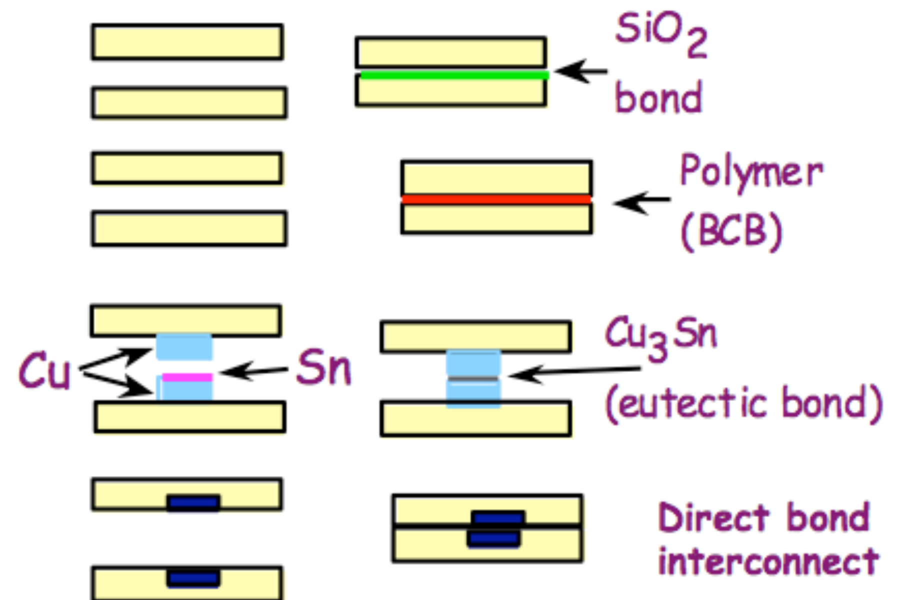
- Silicon on Insulator:
  - Thin active circuit layer on insulating substrate.
    - 200nm of silicon on buried oxide (BOX), carried on handle wafer
  - handle wafer can be high grade silicon- combine electronics and fully depleted detector in single wafer
  - Diode can be formed by implantation through the BOX
  - SOI wafer integrated into 3D concept



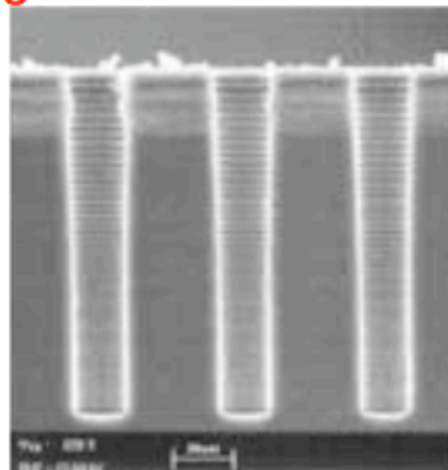
Steps for SOI wafer formation

Key Technologies for SOI/3D

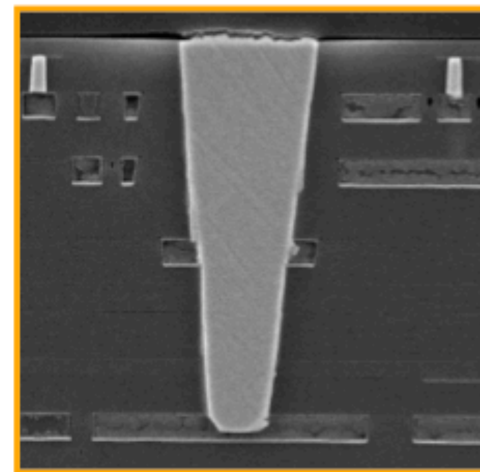
1) Bonding between layers
   - Oxide to oxide fusion
   - Copper/tin bonding
   - Polymer/adhesive bonding
2) Wafer thinning
   - Grinding, lapping, etching, CMP
3) Through wafer via formation and metalization
   - With isolation
   - Without isolation
4) High precision alignment



SEM of 3 vias using Bosch process



Via using oxide etch process (Lincoln Labs)



From R.Lipton
FNAL 2007 Vertex Review

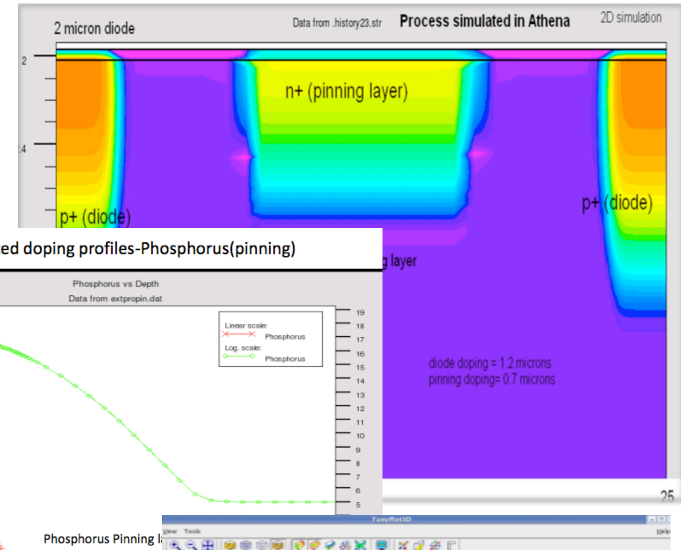
Some R&D issues

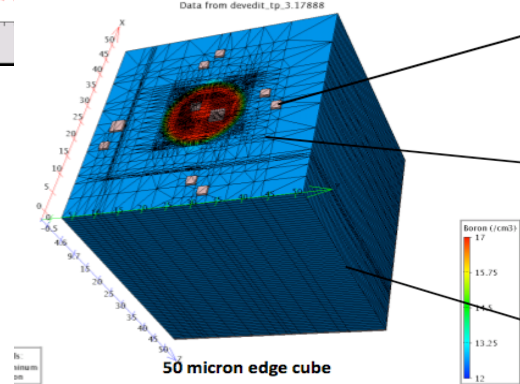
- Explore SOI processes which include handle wafer processing
  - Pursued by FNAL at 3 foundries: OKI, ASI, MIT-LL
  - FNAL designed Vertical Integrated Pixel (VIP) chip for ILC pixel detector, no integrated sensor (yet)
    - MIT-LL and Tezzaron submissions
- Cornell collaborating on some aspects of this work:
  - Modeling of detectors for process optimization
    - charge collection, shielding, …
  - After thinning of devices, a backside contact must be formed
    - implantation of dopants, activation through laser anneal
  - Resources:
    - Cornell Nanoscale Science&Technology Center and Material Science Lab
    - Can get commercial software license at reasonable price

Simulation of sensors

Tool: Silvaco TCAD package (athena, devedit3d, atlas)

- Input: Process parameters (resistivity, implants,..)
- Step 1: Simulation of doping profile (2D)
- Step 2: Doping profile extraction
- Step 3: Device geometry (mesh setup) and doping setup in 3D
- Step 4: Device simulation
  - capacitance measurement
  - Electric potential profile
  - Charge collection efficiency



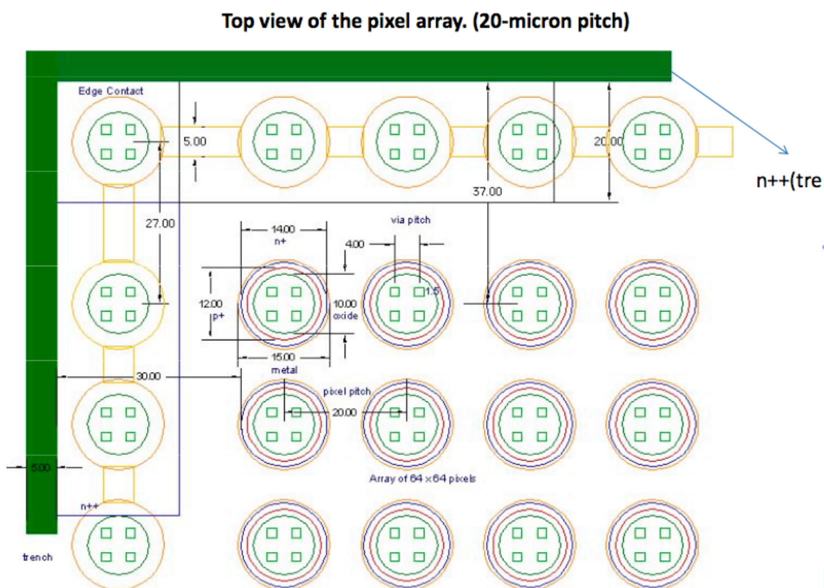


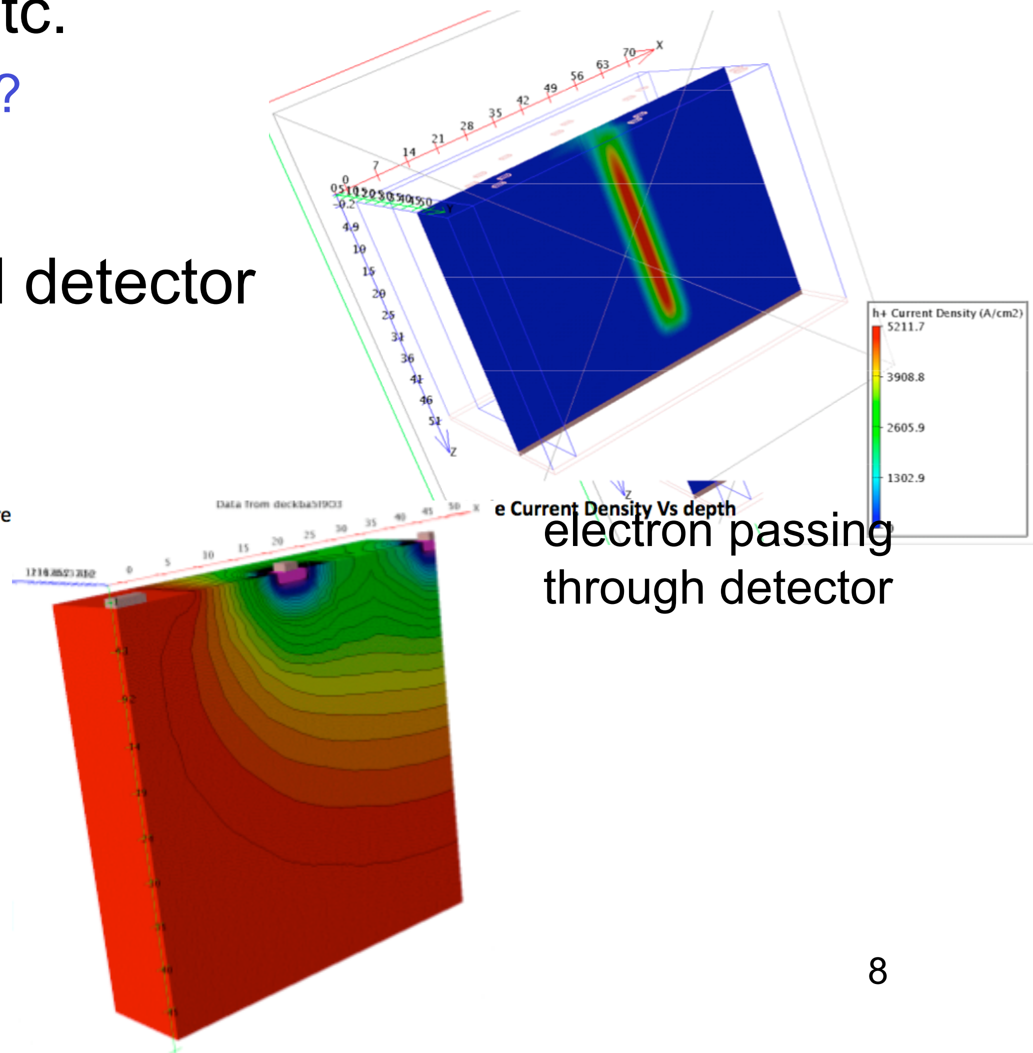
Initial studies on MIT-LL detector by an undergrad

- Will continue with graduate student over summer
- Work on SOI sensor for VIP chip, look into problem of digital coupling into sensor

Simulation of sensors

- Use to study sensor features like pinned diodes, edge trenches, channel stops etc.
  – charge collection efficiency?
  – optimal spacing of diodes?
- Example: “edgeless” pixel detector



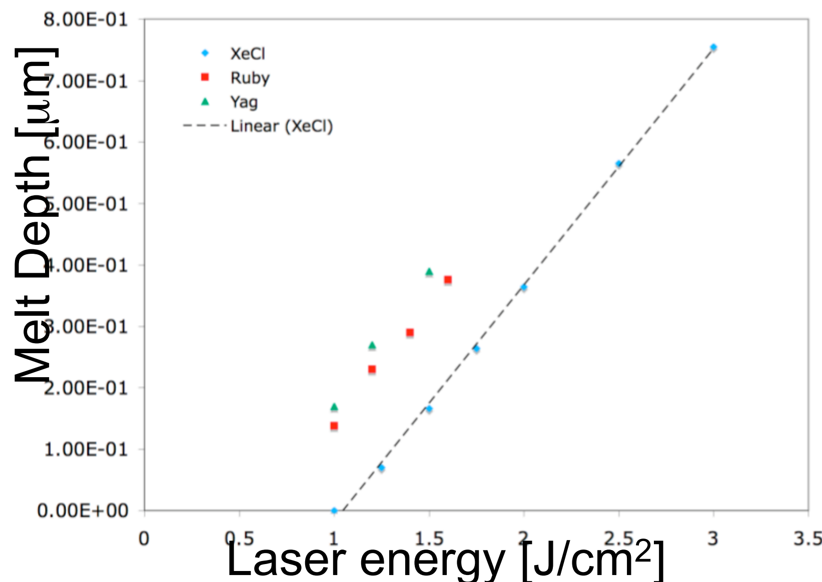


electron passing through detector

Development of backside processing steps

special backside processing needed to avoid damage to front side active circuitry:

1. Thinning to 50-100 μm
2. Implantation of dopants
3. Repair of grinding damage and activation of dopants
   - Formation of extremely low leakage backside junction at end of processing
   - Static temperatures must remain below 400^0C

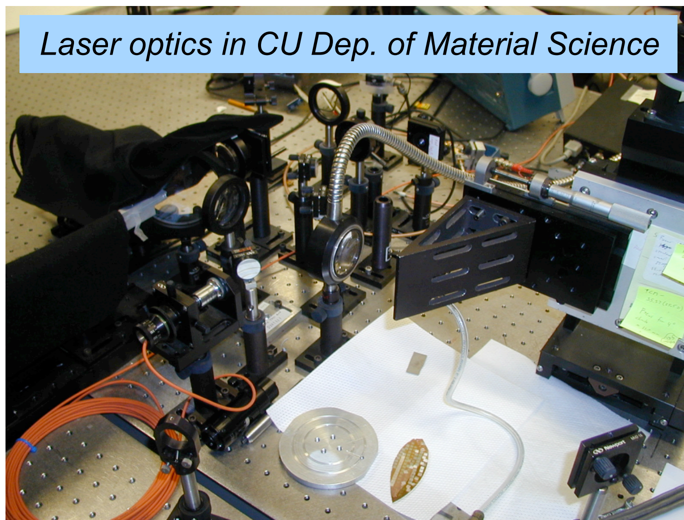


Only technique now: pulsed laser anneal (also used in optical CCDs).
Melt depth for XeCl excimer laser as function of energy (1-1.75 J/cm^2), from
Young et al, IEEE electron device letters, 1982

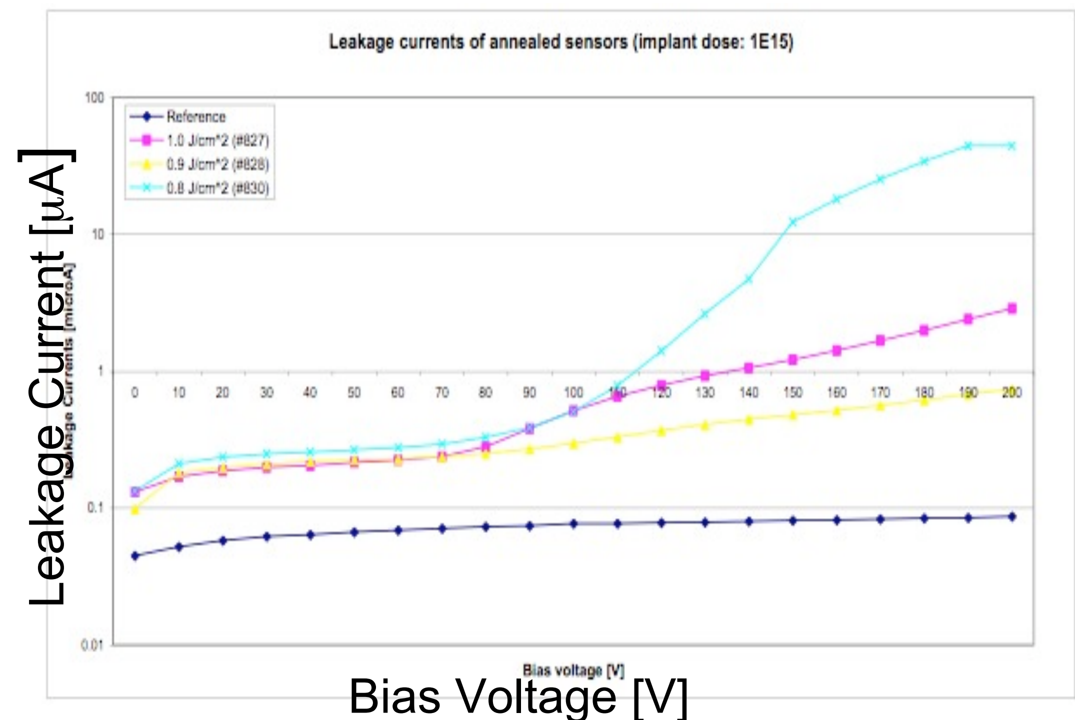
Development of backside processing steps

Care has to be taken to melt deep enough to activate tail of dopant distribution. Tail depends on dopant implant and energy. Initial tests: Run2b D0 microstrip detectors

- thinned and implanted with As/P at 10KeV
- dopant density: 0.5E15/cm^2 and 1E15/cm^2
- laser anneal with XeCl, 0.8 J/cm^2 to 1.27 J/cm^2



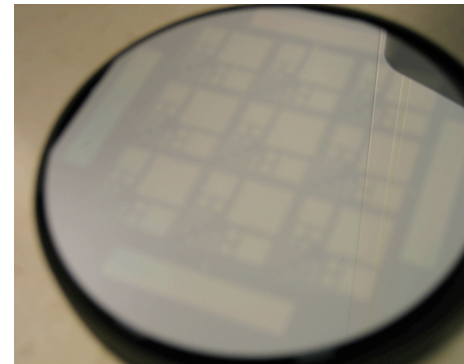
Beam spot 1x1 cm,
uniform exposure, XeCl laser
(308nm; 30ns)

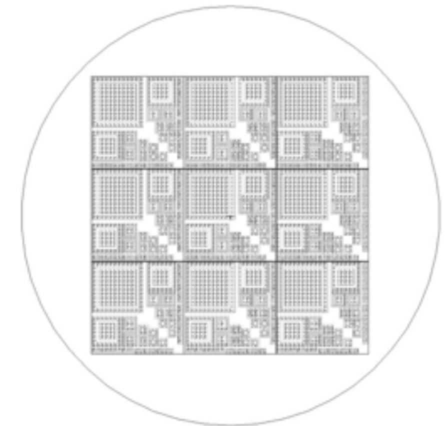


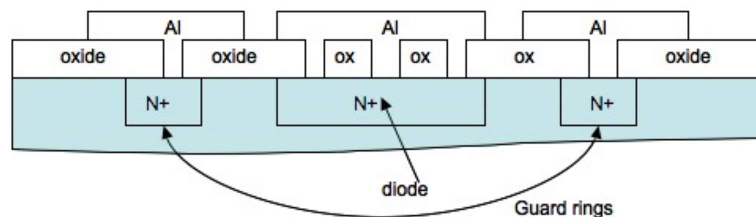
CNF Cornell NanoScale Science and Technology Facility

Fabrication of test diodes to study laser anneal parameters

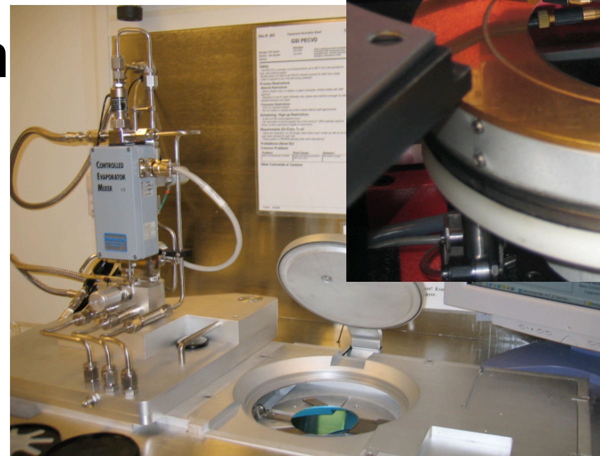
Systematic Study of leakage current as function of implant dose, implant energy, diode size, and laser energy

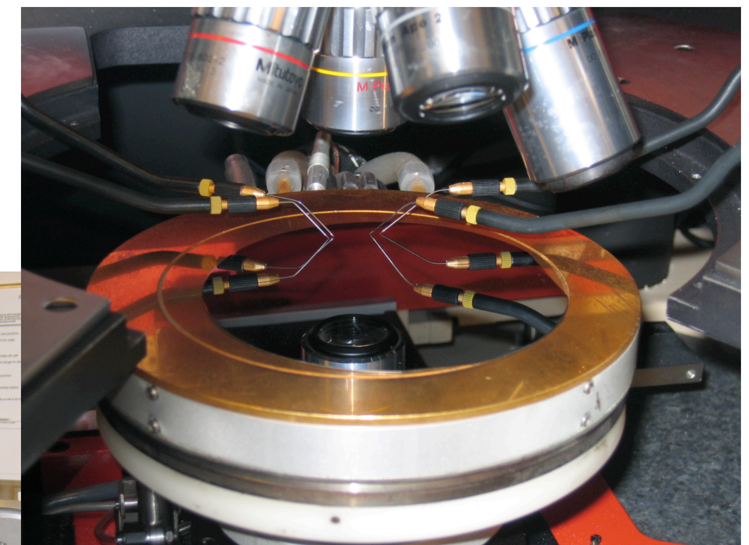






After fabrication, implantation and laser anneal: test wafer is being characterized using a probe station.





Summary

Have been exploring issues related to 3D/SOI devices at Cornell

- Simulations of FNAL design SOI processes
  - Goal: provide feedback to ILC sensor design for demonstration of 3D technology over summer
  - Will start to work on SOI sensor from OKI/KEK
- laser annealing of thinned SOI-based sensors
  - Have developed process to implant and anneal thin sensors at Cornell
  - In process of working on SOI devices from OKI
  - May also be useful for DEPFET sensors

backup

Development of backside processing steps

Testing implant depth profiles by secondary ion mass spectroscopy

Samples before (red) and after (blue) laser anneal (melt depth ~300nm)

Resulting phosphorus concentration close to expectation